Matira7 Title Page/Index

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055	DDR4 DIMM1 CPU1.CHJ.D0	
056	DDR4 DIMM7 CPU1.CHJ.D1	
057	DDR4 DIMM6 CPU1.CHK.D0	
058	DDR4 DIMM12 CPU1.CHK.D1	
059	DDR4 DIMM4 CPU1.CHL.D0	
060	DDR4 DIMM10 CPU1.CHL.D1	
061	DDR4 DIMM2 CPU1.CHM.D0	
062	DDR4 DIMM8 CPU1.CHM.D1	
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064	CPU Common Logic - 1OF2	LOGIC
065	CPU Common Logic - 2OF2	
066	Clock Buffer - 1OF2	CLOCK
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068	PCIE G3 X8 - Slot1_CPU0	PCIE SLOT
069	PCIE G3 X16 - Slot2_CPU0	
070	PCIE G3 X16 - Slot4_CPU0	
071	PCIE G3 X16 - Slot6_CPU1	
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076	PCH CLOCK/Mlisc/JTAG	PCH
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089	GBE I219 Jacksonville_LOM1	LAN
090	GBE I210 Springville_LOM2	
091	Blank	
092	Audio Codec	AUDIO
093	Audio Connector	
094	USB 3.0 Connector - 1OF3	USB
095	USB 3.0 Connector - 2OF3	
096	Front Panel USB3_1	
097	INT USB 2.0	
098	Front Panel USB3_2	
099	USB 3.0 Connector - 3OF3	
100	Blank	
101	Blank	
102	PCH_FIX- IO Storage Connector	STORAGE
103	PS/2 KBMS/Serial	PS/2
104	Power Conn/Front Panel	CONN
105	Fan Conector_1	FAN
106	Fan Conector_2	
107	TPM/SPI ROM	TPM/SPI
108	Debug/Label/Misc	XDP
109	MERGED XDP - DCI	DCI
110	SMBUS MUX	SMBUS
111	OTHER	OTHER
112	VR, CPU0 CORE CONTROLLER	CPU0 VR
113	VR, CPU0 CORE OUTPUT	
114	VR, CPU0_VCCSA OUTPUT	
115	VR, CPU0_VCCIO CONTROLLER	
116	VR, CPU0_VCCIO OUTPUT	
117	BLANK	
118	BLANK	
119	BLANK	
120	VR, CPU1 CORE CONTROLLER	CPU1 VR
121	VR, CPU1 CORE OUTPUT	
122	VR, CPU1_VCCSA OUTPUT	
123	VR, CPU1_VCCIO CONTROLLER	
124	VR, CPU1_VCCIO OUTPUT	
125	BLANK	
126	BLANK	
127	BLANK	
128	VR, CPU0_VDDQ012_PWM	CPU0 MEM VR
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P.	Contents	Function
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134	VR, CPU1_VDDQ345_PWM	
135	VR, CPU1_VDDQ345_OUT	
136	VR, MEMORY VPP_CPU0	MEM VPP
137	VR, MEMORY VPP_CPU1	
138	VR, MEMORY VTT	MEM VTT
139	VR, PVNN CONTROLLER	SYS VR
140	VR, +1P05V/+1P8V/+PGPPA	
141	LOADSWITCH, +5V/+3P3V	LOAD SWITH
142	+3P3V_DSW/+5V_AUX/+3P3V_SLOT	
143	VR, 3.3_AUX,+5V_USBKB, V_3/5VAUX_MEM_CPU0/1	
144	+P2V5_CPU0/1	MEM VR
145	Blank	
146	Changelist_A	
147	Changelist_B	
148	Changelist_C	
149	Changelist_D	
150	Changelist_E	

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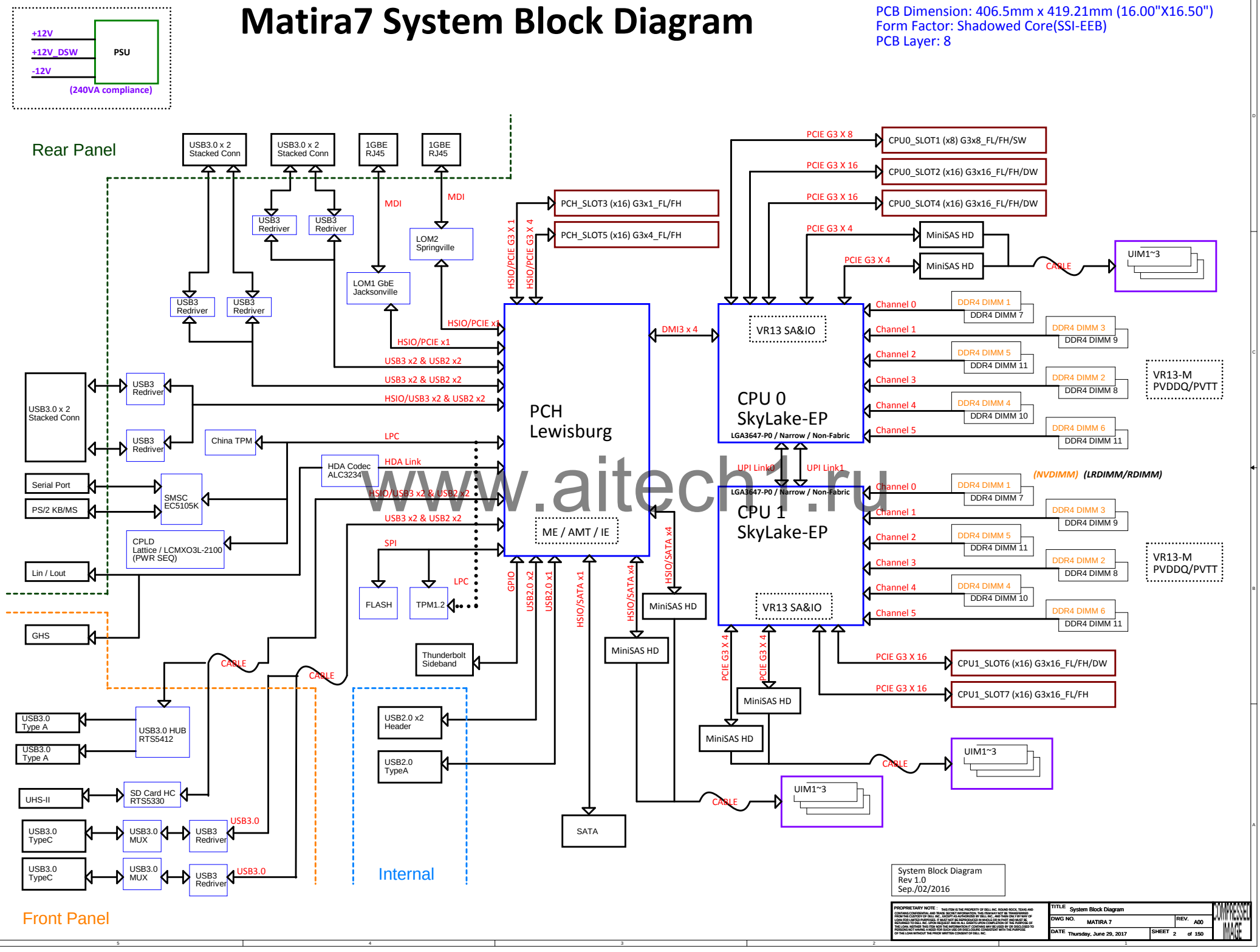
COMPRESSED IMAGE

Matira7 System Block Diagram

PCB Dimension: 406.5mm x 419.21mm (16.00"X16.50")
Form Factor: Shadowed Core(SSI-EEB)
PCB Layer: 8



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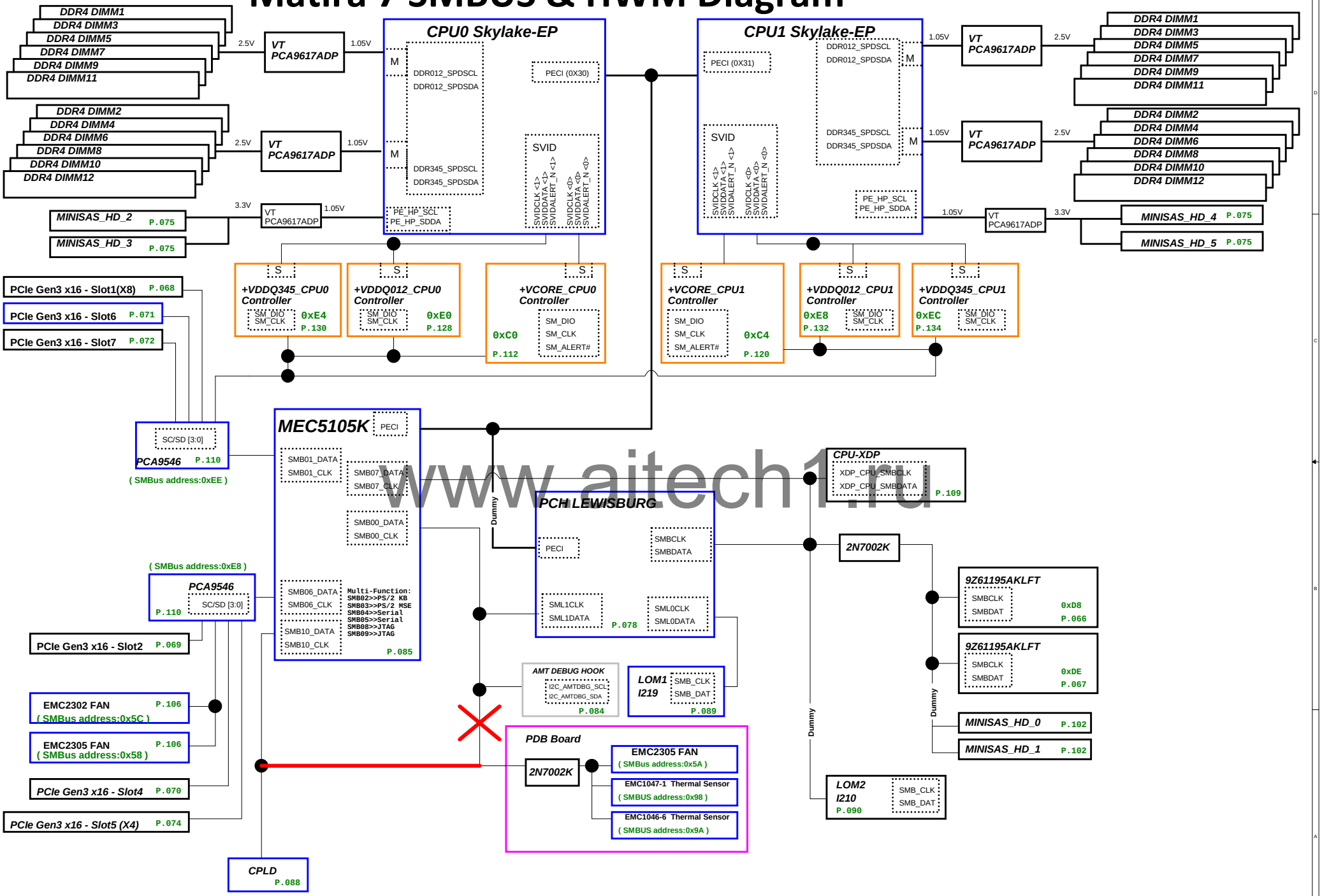
Matira 7 SMBUS & HWM Diagram



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SMBUS & HWM Map
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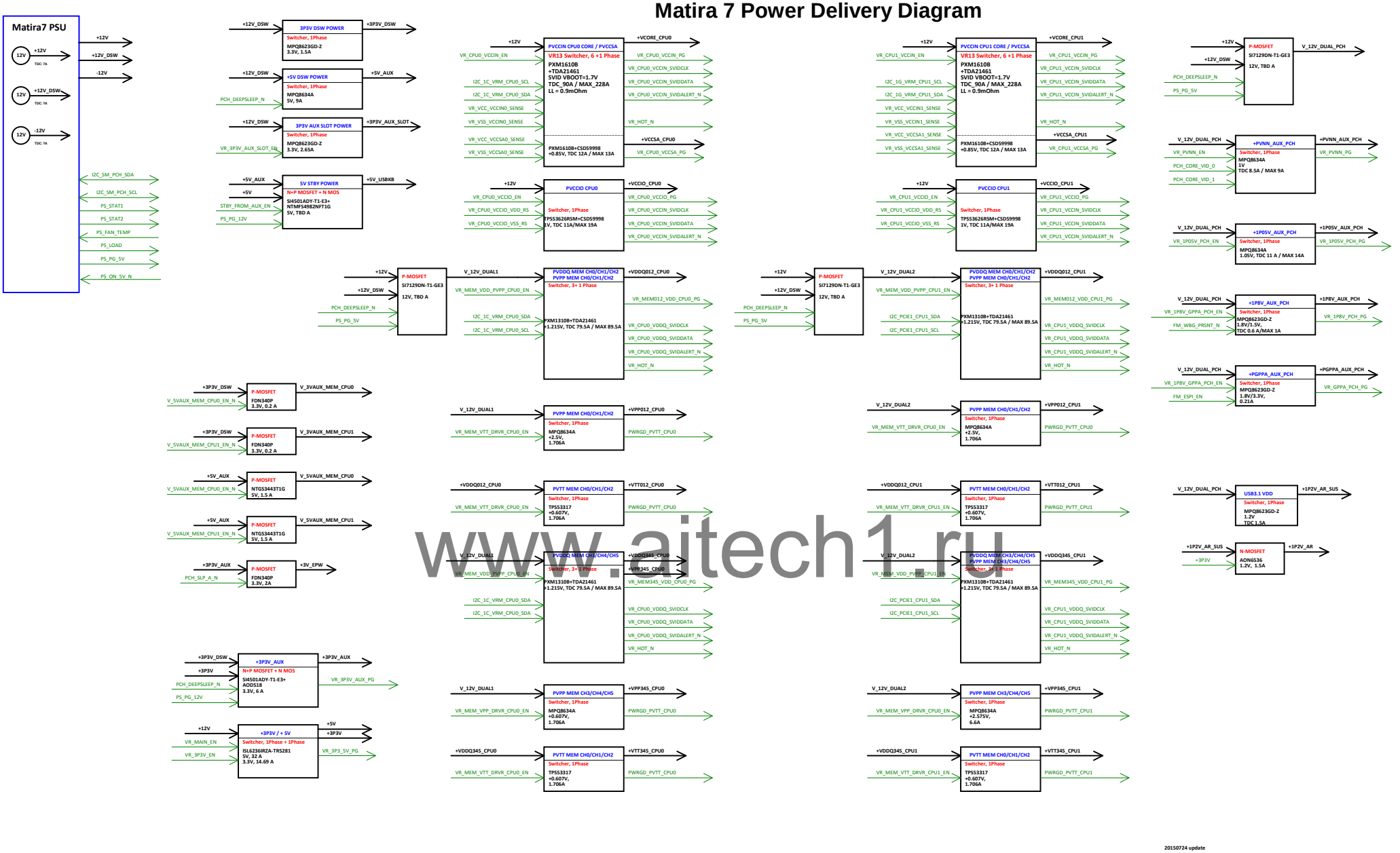
Matira 7 Power Delivery Diagram



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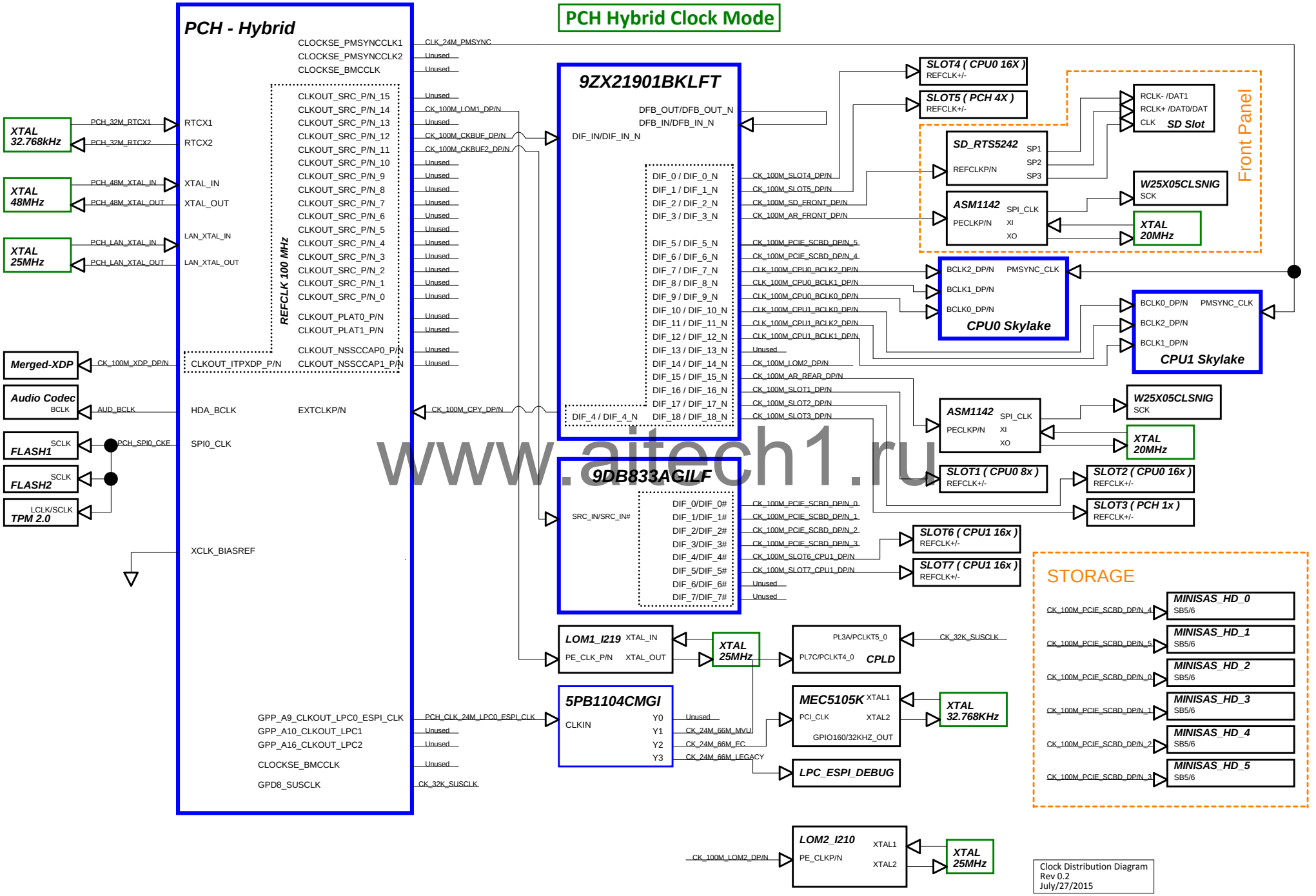
Matira7 Clock Distribution Diagram



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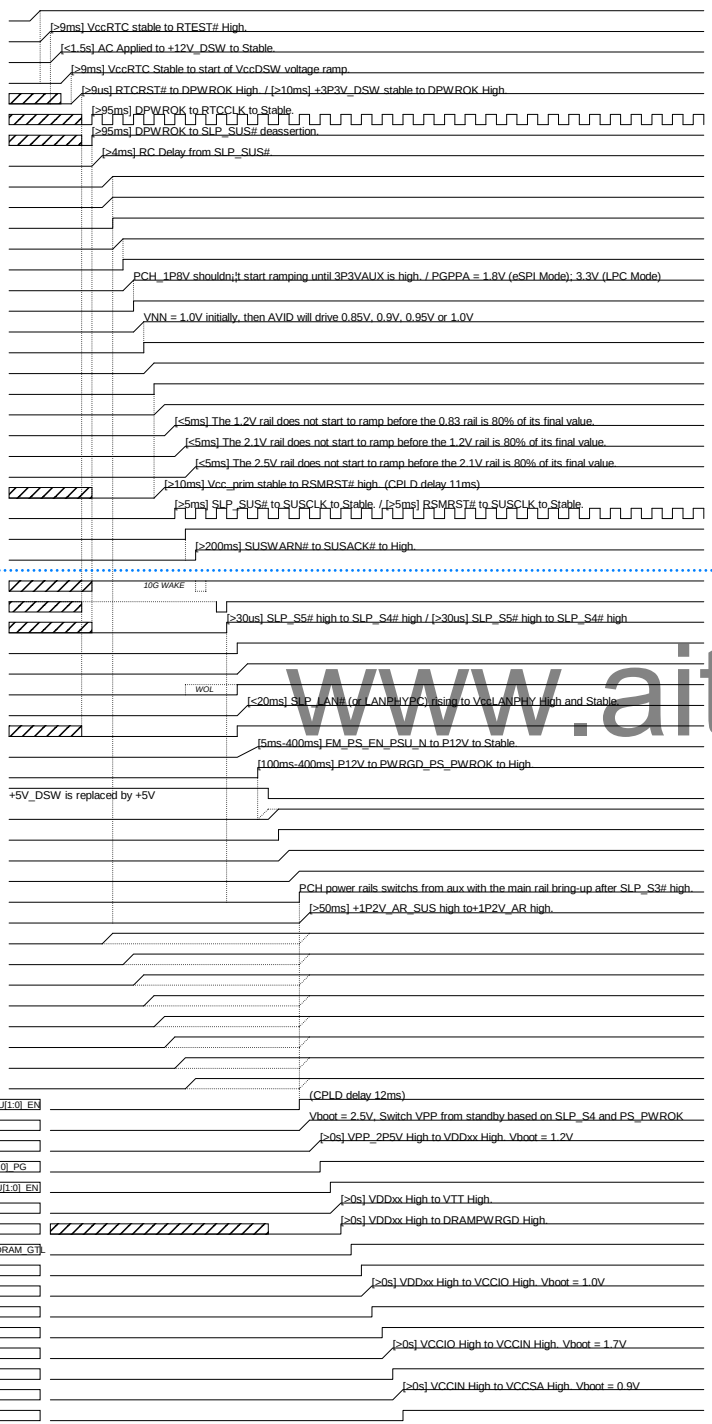
COMPRESSED IMAGE

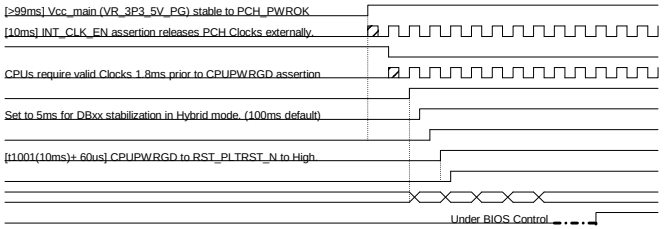
Matira7 Power Sequence Diagram

G3 to S5 / S5 to S0 Timing Diagram

Source	Destination	Signal_Name
Board	PCH	V_3V_VBAT
Board	PCH	PCH_RTCRST_N
PSU	Board	+12V_DSW
Board	PCH	+5V_DSW / +3P3V_DSW
Board	PCH	VR_PCH_DSW_PWROK
Board	PCH	PCH_32M_RTCX[2:1]
PCH	CPLD / EC / VR	PCH_DEEPSLEEP_N
VR	VR	V_12V_DUALx_MEMx
VR	ASM1142	+1P2V_AR_SUS
VR	Board	+3P3VAUX
CPLD / EC	VR	VR_3P3V_AUX_SLOT_EN
VR	Board	+3P3V_AUX_SLOT
CPLD / EC	VR	VR_1P8V_GPPA_PCH_EN
VR	Board	+1P8V_AUX_PCH (+PGPPA_AUX_PCH)
CPLD / EC	VR	VR_PVNN_EN
VR	Board	+PVNN_AUX_PCH
CPLD / EC	VR	VR_1P05V_PCH_EN
VR	Board	+1P05V_AUX_PCH
VR	Board	VR_1P05V_PCH_PG
VR	LOM2	+VDD0P83_AUX_LOM2
VR	LOM2	+VCC1P2_AUX_LOM2
VR	LOM2	+VCC2P1_AUX_LOM2
VR	LOM2	+VDD2P5_AUX_LOM2
EC5055	PCH	PCH_RSMRST_N
PCH	CPLD	CK_32K_SUSCLK
PCH	Board (CPLD / EC)	PCH_SUSWARN_N
Board	PCH	PCH_SUSACK_N
PCH	Board	PCH_WAKE_N
Board	PCH / CPLD / EC	PCH_PWRBTN_N
PCH	Board / CPLD / EC	PCH_SLP_S[5,4,3]_N
PCH	Board / CPLD / EC	PCH_SLP_A_N
VR	Board	+3V_EPW
PCH	VR	PCH_SLP_LAN_N
VR	LOM1	+3P3V_DSW_LAN
CPLD / EC	PSU	PS_ON
PSU	Board	+12V
PSU	Board / CPLD / EC	PS_PG_12V (PS_PG_3P3_N)
CPLD / EC	Board	STBY_FROM_AUX_EN
VR	Board	+5V_USBKB
CPLD / EC	VR	VR_MAIN_EN (VR_3P3V_EN)
VR	Board	+5V
VR	Board	+3P3V
VR	Board	VR_3P3_5V_PG
VR	Board	+1P2V_AR
VR	PCH	+3P3VAUX
VR	PCH	+1P8V_AUX_PCH (+PGPPA_AUX_PCH)
VR	PCH	+PVNN_AUX_PCH
VR	PCH	+1P05V_AUX_PCH
VR	LOM2	+VDD0P83_AUX_LOM2
VR	LOM2	+VCC1P2_AUX_LOM2
VR	LOM2	+VCC2P1_AUX_LOM2
VR	LOM2	+VDD2P5_AUX_LOM2
CPLD / EC	VR	VR_MEM_VDD_PVPP_CPU[1:0]_EN
VR	DRAM / CPU	+VPP[012,345]_CPU[1:0]
VR	DRAM / CPU	+VDDQ[012,345]_CPU[1:0]
VR	EC / CPLD	VR_MEM[5:0]_VDD_CPU[1:0]_PG
CPLD / EC	VR	VR_MEM_VTT_DRVR_CPU[1:0]_EN
VR	DRAM	+VTT[012,345]_CPU[1:0]
CPLD / EC	Board	CPU_MEM_VDD_PG
Board	CPU	PWRGD_CPU[1:0]_[M:A]_DRAM_GT
CPLD / EC	VR	VR_CPU[1:0]_VCCIO_EN
VR	CPU	+VCCIO_CPU[1:0]
VR	CPLD / EC	VR_CPU[1:0]_VCCIO_PG
CPLD / EC	VR	VR_CPU[1:0]_VCCIN_EN
VR	CPU	+VCORE_CPU[1:0]
VR	CPLD / EC	VR_CPU[1:0]_VCCIN_PG
VR	CPU	+VCCSA_CPU[1:0]
VR	CPLD / EC	VR_CPU[1:0]_VCCSA_PG



Source	Destination	Signal_Name
CPLD / EC	PCH	PCH_PWROK_PG
PCH	Board	PCH isClocks
CPLD / EC	DB1x00Z	CLK_CPU_BCLKS_EN_N
DB1x00Z	Board	DB1x00Z Clocks
PCH	CPLD / EC	PCH_PROC_PWRGD
CPLD / EC	CPU	CPLD_PROC_PWRGD
CPLD / EC	PCH	PCH_SYS_PWROK
PCH	CPLD / EC	PCH_PLTRST_N
CPLD / EC	Board	PERST#
CPU	CPLD / EC	H_CPU[1:0]_FIVR_FAULT_GTL
CPU	DRAM	M_xxx_RESET_N



S0 to S5 Timing Diagram

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Power Sequence Diagram
Rev 0.1
July/28/2015

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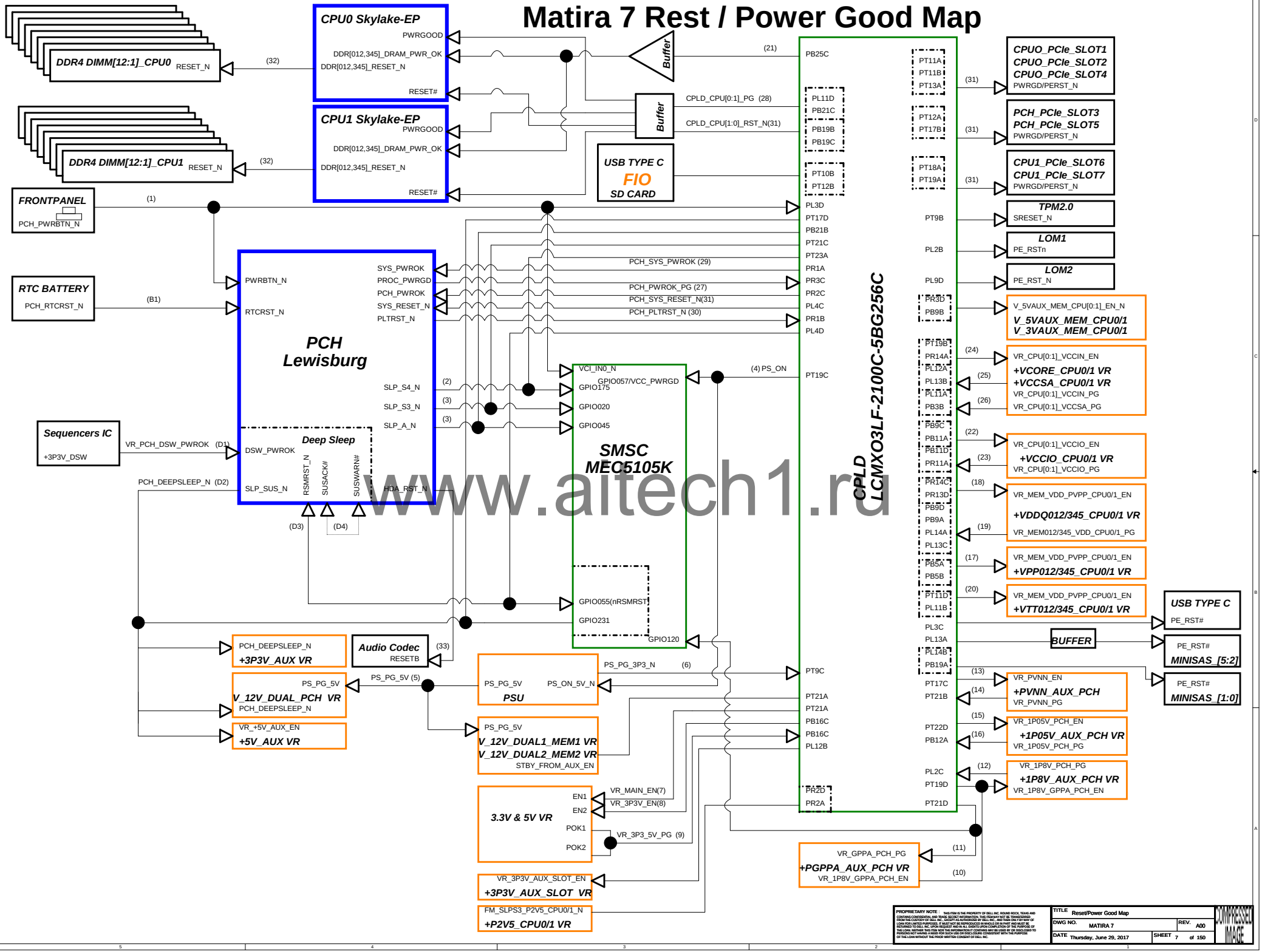
COMPRESSED IMAGE

Matira 7 Rest / Power Good Map



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TITLE	Reset/Power Good Map
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Matira 7 Strap/IRQ/IDSel Table

PCH Functional Strap

Signal	Usage	When Sampled	Comment
GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit 10 — Boot BIOS Destination** 0 — SPI 1 — LPC/eSPI ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC/eSPI) is selected, BIOS may still be placed on LPC/eSPI but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or LAN.
GPP_C5_SML0ALERT_IE#	eSPI_EN	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** functionality is selected. 1 = **eSPI** functionality is selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts.
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
GPP_H12_SML2ALART_IE# /	Master or Slave Attached Flash	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master attached Flash. 1 = Slave Attached Flash. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts.
GPP_H15	ADR Timer Hold Off	RSMRST	This signal has a weak internal pullup. 0 = ADR Timer Hold off is enabled. 1 = ADR Timer Hold off is not enabled.
GPP_K9_LAN_NCSI_ARB_OUT	LAN Aux Power	rising edge of Global Reset (find pin)	This signal has a weak internal pull-down. 0 = D3COLD is not supported. 1 = Aux power is available and the 10Gbe LAN should support the D3COLD power state if enabled to do so.
SPI_MISO	SPI Buffer voltage	rising edge of RSMRST#	If sampled low, then SPI buffer is set to 1.8V. If high, then the buffer is 3.3V
GPP_H18_SML4ALERT_N_IE_N	RSVD	rising edge of RSMRST#	This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#
GPP_K7	RSVD	rising edge of RSMRST#	This pin has an internal pulldown. This strap needs to be sampled low during the rising edge of RSMRST#

Signal	Usage	When Sampled	Comment
SPIO_MOSI	RSVD	rising edge of RSMRST#	This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#
GPP_B23_MEI-E_SML1AL-RT_N_PHOT_N	DCI Enable	rising edge of RSMRST#	This pin has an internal pulldown. This strap needs to be sampled low during the rising edge of RSMRST#
SPIO_IO_2	RSVD	rising edge of RSMRST#	This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#
SPIO_IO_3	RSVD	rising edge of RSMRST#	This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#

Signal	Usage	When Sampled	Comment
GPP_B14_SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address bit (defined in FITC) at the top of system BIOS space. This provides an alternate physical address that the processor accesses at boot. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4).
GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running Intel® ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5).
GPP_C2_SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel® Small Business Advantage (Intel® SBA) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts.

PCH IRQ

Name	Type	Description
GPP_A6_SERIRQ_ESPI_CS1#	I/O	Serial Interrupt Request ***Note:*** An external pull-up is required
GPP_A7_PIRQA#_ESPI_ALERT0#	I/OD	PCI Interrupt Request A ***Note:*** Note: An external pull-up is required

CPU Functional Strap

Signal Name	Description
BIST_ENABLE	BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. Refer to Table 2-8 for details.
BMCINIT	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs. 0: Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it) 1: Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a "GO" handshake signal via a firmware scratchpad register. This signal is pulled down on the die, refer to Table 2-8 for details. For further details see *Skylake Server External Design Specification (EDS), Volume One: Architecture*
DMIMODE_OVERRIDE	BMCINIT, DMIMODE_OVERRIDE, FRMAGENT, and LEGACY_SKT, whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe.
SAFE_MODE_BOOT	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 2-8 for details.
FRMAGENT	Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). The firmware flash ROM is located behind the local PCH attached to the processor via the DMI3 interface.This signal is pulled down on the die, refer to Table 2-8 for details. For further details see *Skylake Server External Design Specification (EDS), Volume One: Architecture.*
PM_FAST_WAKE_N	Power Management Fast Wake. Enables quick package C3 - C6 exits of all sockets. Asserted if any socket detects a break from package C3 - C6 state requiring all sockets to exit the low power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform.
PROC_ID [1:0]	This output can be used by the platform to determine if the installed processor is a Skylake Server, Cannonlake Server, or a future processor planned for Purley. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. 00: Skylake Server 01: Cannonlake 10: Reserved 11: Reserved.
SOCKET_ID[2:0]	SOCKET_IDStrap. Socket identification configuration straps for establishing the PECI address and Intel UPI Node ID. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 2-8 for details. For further details see *Skylake Server External Design Specification (EDS), Volume One: Architecture* SOCKET_ID[1:0] is used for 2S platforms and SOCKET_ID[2:0] is implemented on 4S/8S platforms. This is an asynchronous signal to other clocks in the processor. Refer to the Platform Design Guide for details.
TXT_AGENT	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die, refer to Table 2-8 for details. For further details see *Skylake Server External Design Specification (EDS), Volume One: Architecture*
TXT_PLTEN	Intel Trusted Execution Technology (Intel TXT) Platform Enable Strap. 0 = The platform is not Intel TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel TXT. 1 = Default. The platform is Intel TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel TXT functionality requires user to explicitly enable Intel TXT via BIOS setup. This signal is pulled up on the die, refer to Table 2-8 for details. For further details see *Skylake Server External Design Specification (EDS), Volume One: Architecture*
LEGACY_SKT	BMCINIT, FRMAGENT, LEGACY_SKT together determine the boot mode (SSP, Intel UPI Link boot modes, DCF boot), whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe (Gen1/2. With one exception, this input configuration strap indicates to the processor that it is the legacy socket. The legacy SKT must be strapped for NODE ID 0, via the SKIT ID pins. There is only 1 legacy SKT in a partition.
PKGID[2:0]	An indicator to the Purley platform of the Intel OmniPath configuration.
SOCKET_ID2	Asynchronous to other clocks in the processor.

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Strap/IRQ/IDSel Table
Rev 0.1
July/30/2015

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TITLE: Strap/IRQ/IDSel Table
DWG NO.: MATIRA 7
REV: ADD
DATE: Thursday, June 29, 2017
SHEET: 8 of 150

Matiral 7 GPIO Table (1 of 2)

PCH WELLSBURG
MEC5055

GPIO Table (1 of 2)
Rev 0.5
Feb/24/2014

- To Be Updated -

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TITLE	GPIO Table - 1OF2		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	9 of 150

COMPRESSED IMAGE

Matiral 7 GPIO Table (1 of 2)

MEC5055 (Cont.)
ECE5048

GPIO Table (2 of 2)
Rev 0.5
Feb/24/2014

-To Be Updated -

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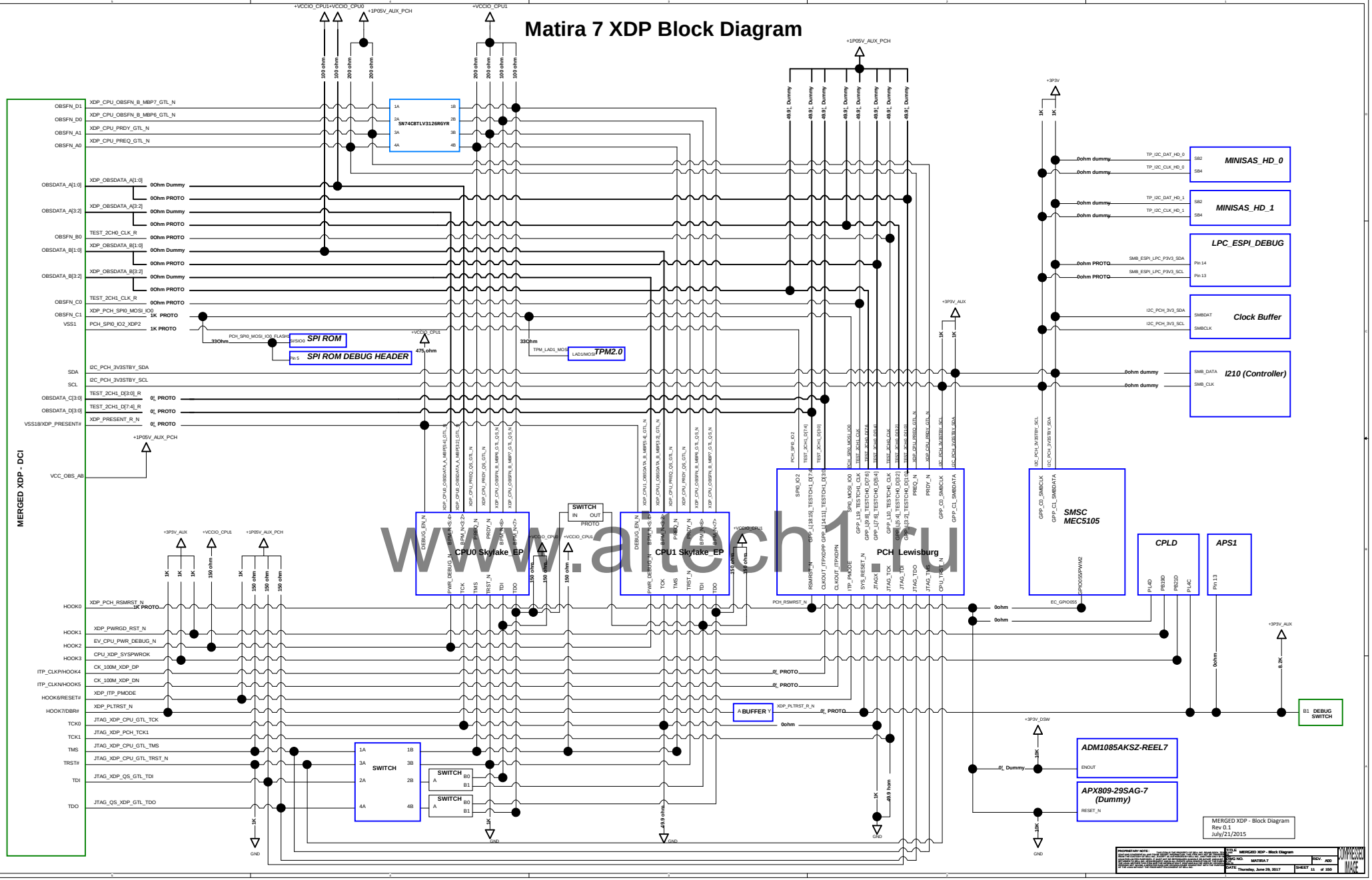
TITLE	GPIO Table - 2OF2		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	10 of 150

COMPRESSED IMAGE

Matira 7 XDP Block Diagram



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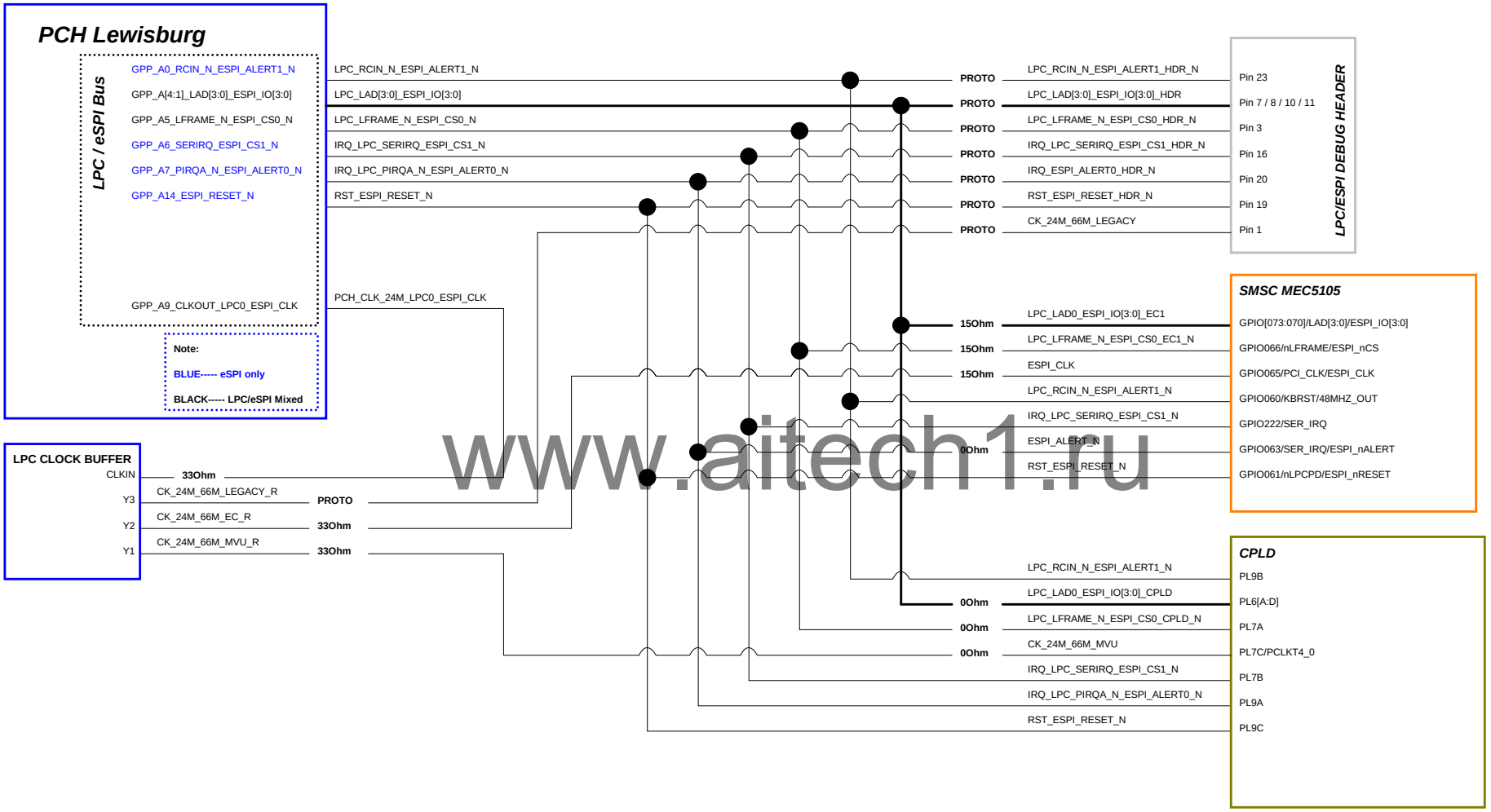
Matira 7 LPC/eSPI Block Diagram



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LPC/eSPI Block Diagram
Rev 0.2
July/27/2015

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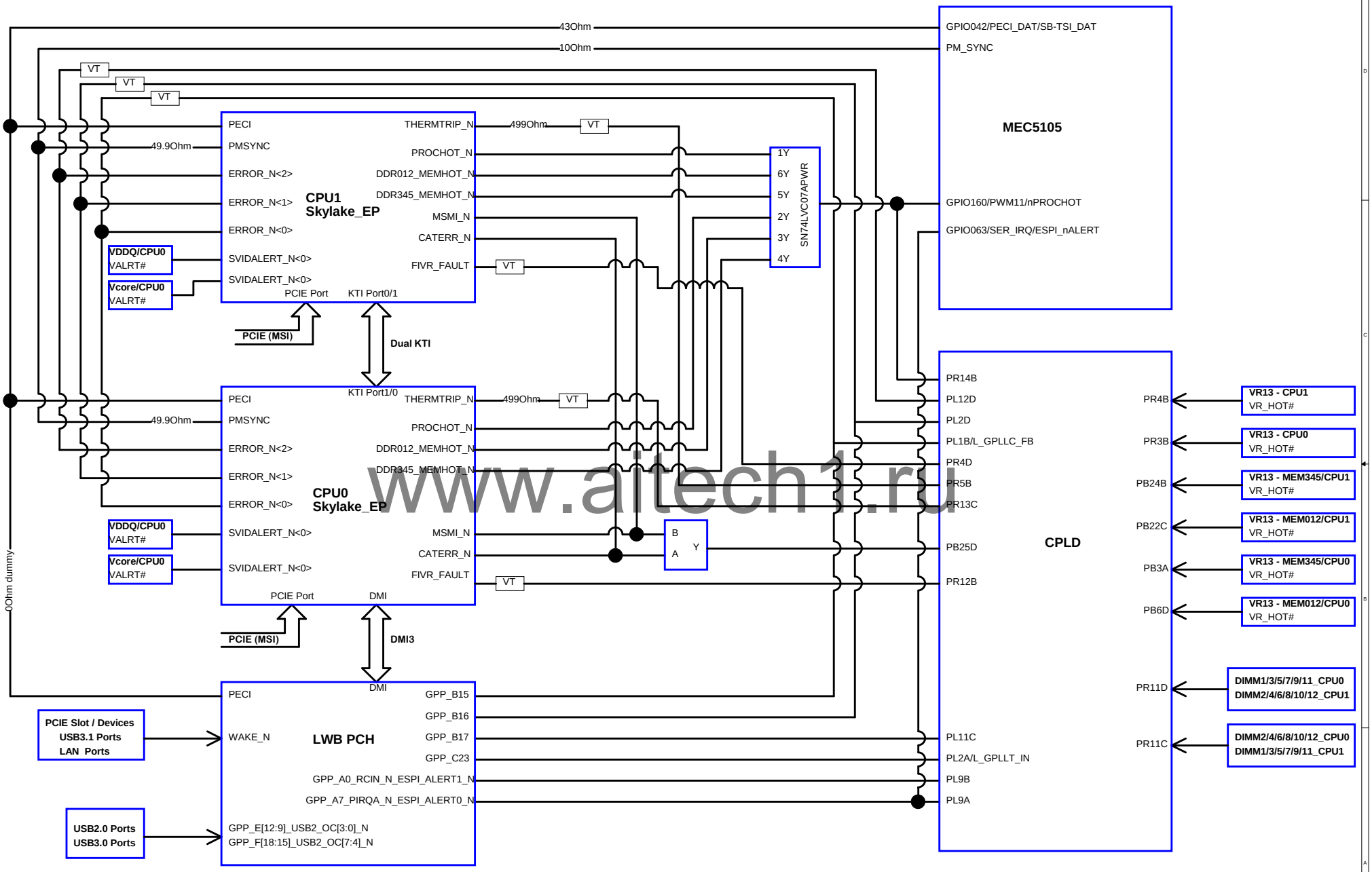
TITLE	Matira 7 LPC/eSPI Block Diagram
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	12 of 150

COMPRESSED IMAGE

Matira 7 Error Management Block Diagram

Error Management Block Diagram
Rev 0.2
June/28/2013



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TITLE	Error Management Diagram
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	13 of 150

COMPRESSED IMAGE

Matira 7 System Power Rail

No.	Power Rails	Voltage	S0	M3		Moff	DSW	G3	Source	Control Signal
				S3	S4/S5					
1	V_3V_VBAT	3V	ON	ON	ON	ON	ON	ON	RTC Battery	RTC Battery
2	+12V_DSW	12V	ON	ON	ON	ON	ON	OFF	PSU	Adaptor in
3	+3P3V_DSW	3.3V	ON	ON	ON	ON	ON	OFF	+12V_DSW	Adaptor in
4	V_12V_DUAL1/2_MEM1/2	12V	ON	ON	ON	ON	ON	OFF	+12V/+12V_DSW	STBY_FROM_AUX_EN/PS_PG_5V
5	V_12V_DUAL_PCH	12V	ON	ON	ON	ON	OFF	OFF	+12V/+12V_DSW	PCH_DEEPSLEEP_N/PS_PG_5V
6	+5V_AUX	5V	ON	ON	ON	ON	OFF	OFF	+12V_DSW	PCH_DEEPSLEEP_N
7	+3P3V_AUX_SLOT	3.3V	ON	ON	ON	ON	OFF	OFF	+12V_DSW	VR_3P3V_AUX_SLOT_EN
8	+3P3V_AUX	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V/+3P3V_DSW	PCH_DEEPSLEEP_N/AUX_FROM_MAIN_12V
9	+1P8V_AUX_PCH	1.8V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_1P8V_GPPA_PCH_EN
10	+PGPPA_AUX_PCH	3.3V/1.8V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_1P8V_GPPA_PCH_EN
11	+PVNN_AUX_PCH	1V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_PVNN_EN
12	+1P05V_AUX_PCH	1.05V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_1P05V_PCH_EN
13	+3P3V_DSW_LAN	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V_DSW	PCH_SLP_LAN_N
14	+1P2V_AR_SUS	1.2V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	V_12V_DUAL_PCH
15	V_3VAUX_MEM_CPU0/1	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V_DSW	V_5VAUX_MEM_CPU0/1_EN_N
16	V_5VAUX_MEM_CPU0/1	5V	ON	ON	ON	ON	OFF	OFF	+5V_AUX	V_5VAUX_MEM_CPU0/1_EN_N
17	+5V_USBKB	5V	ON	ON	OFF	OFF	OFF	OFF	+5V/+5V_AUX	STBY_FROM_AUX_EN /AUX_FROM_MAIN_12V
18	-12V	-12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON
19	+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON
20	+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	+12V	VR_MAIN_EN
21	+3P3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	+12V	VR_3P3V_EN
22	+VDDQ012/345_CPU0/1	1.2V	ON	OFF	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	VR_MEM_VDD_PVPP_CPU0/1_EN
23	+VPP012/345_CPU0/1	2.5V	ON	OFF	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	MEM_VPP012/345_CPU0/1_EN_R
24	+VTT012/345_CPU0/1	0.6V	ON	OFF	OFF	OFF	OFF	OFF	+VDDQ012/345_CPU0/1	MEM_VTT_DRVR_CPU0/1_EN
25	+VCORE_CPU0/1	1.8V	ON	OFF	OFF	OFF	OFF	OFF	+12V	VR_CPU0/1_VCCIN_EN
26	+VCCSA_CPU0/1	0.85V	ON	OFF	OFF	OFF	OFF	OFF	+12V	VR_CPU0/1_VCCIN_EN
27	+VCCIO_CPU0/1	1V	ON	OFF	OFF	OFF	OFF	OFF	+12V	VR_CPU0/1_VCCIO_EN
28	+P2V5_CPU0/1	2.5V	ON	OFF	OFF	OFF	OFF	OFF	+VPP012_CPU0/1	FM_SLPS3_P2V5_CPU0/1_N
29	+1P2V_AR	1.2V	ON	OFF	OFF	OFF	OFF	OFF	+1P2V_AR_SUS	+3P3V
30	+1P5V_AVDD	1.5V	ON	OFF	OFF	OFF	OFF	OFF	+3P3V	+3P3V

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System Power Rail
Rev 0.2
July/27/2015

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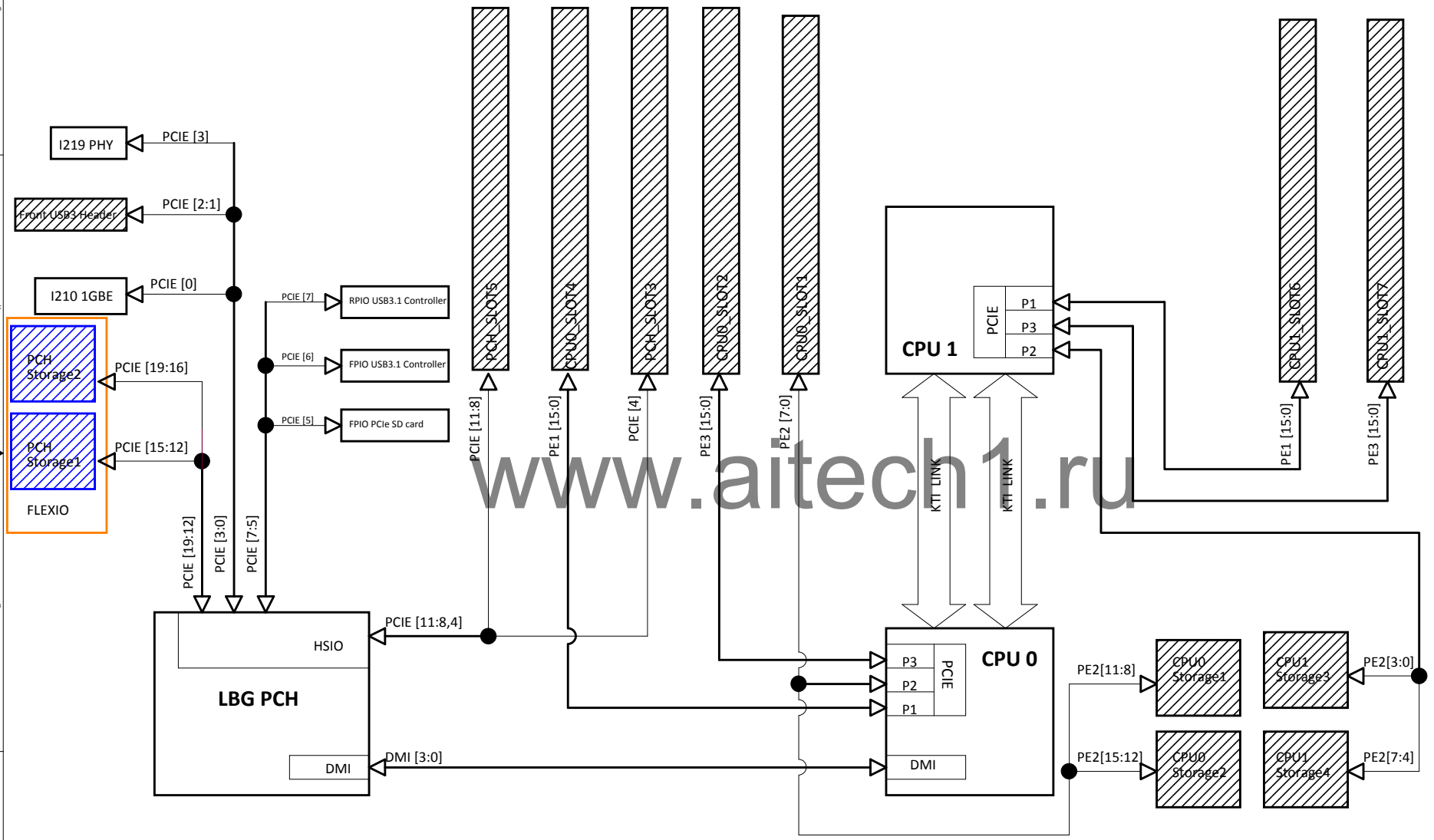
TITLE	System Power Rail
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	14 of 150

COMPRESSED IMAGE

Matira 7 PCIe Connection Diagram



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PCIe Connection Diagram
Rev 0.2
July/23/2015

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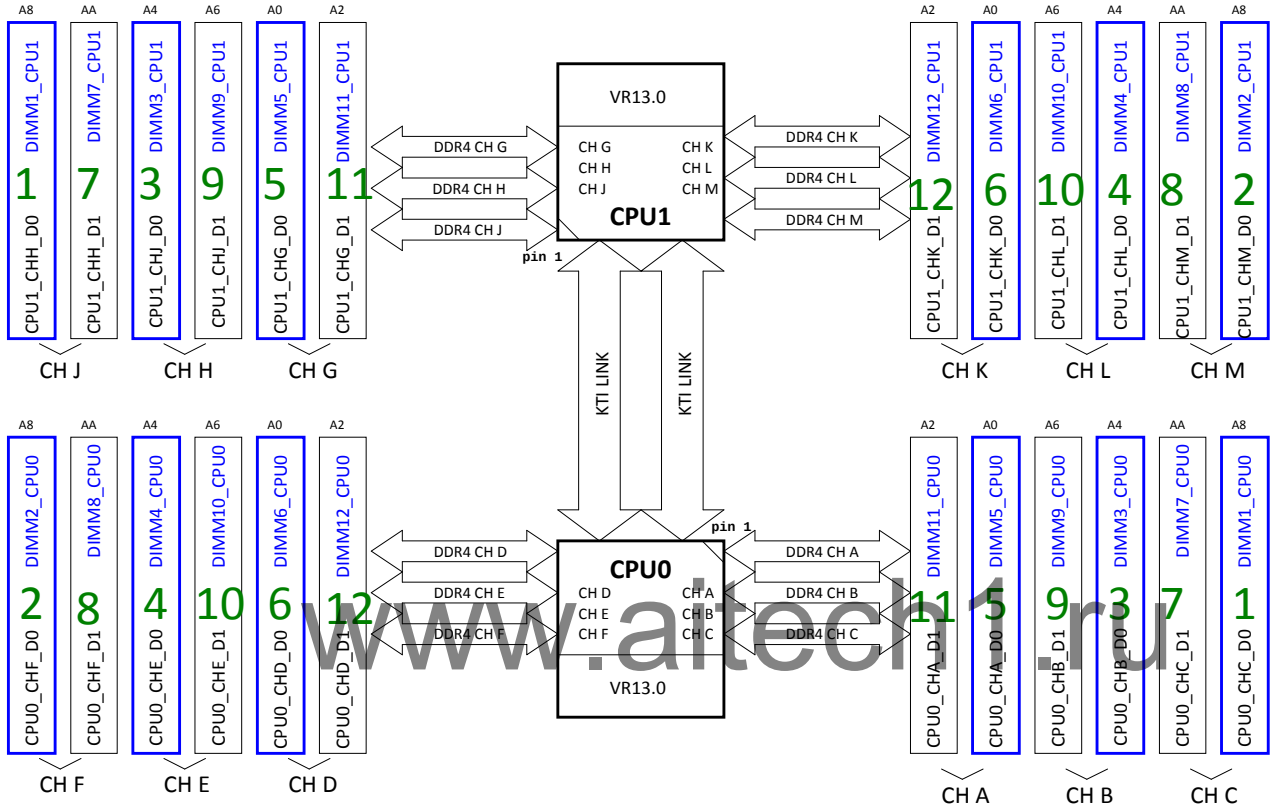
TITLE	PCIe Connection Diagram
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	15 of 150

COMPRESSED IMAGE

Matira 7 Memory Connection Diagram



White Ejector / Black Body

Black Ejector / Black Body

SILKSCREEN	CHANNEL	DIMM	SA[2:0]	SPD	TSOD
DIMM1	C	0	100	0xA8	0x38
DIMM7		1	101	0xAA	0x3A
DIMM3	B	0	010	0xA4	0x34
DIMM9		1	011	0xA6	0x36
DIMM5	A	0	000	0xA0	0x30
DIMM11		1	001	0xA2	0x32
DIMM2	F	0	100	0xA8	0x38
DIMM8		1	101	0xAA	0x3A
DIMM4	E	0	010	0xA4	0x34
DIMM10		1	011	0xA6	0x36
DIMM6	D	0	000	0xA0	0x30
DIMM12		1	001	0xA2	0x32

Memory Connection Diagram
Rev 0.3
2/24/2016

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TITLE Memory Connection Diagram
DWG NO. MATIRA 7
REV. A00
DATE Thursday, June 29, 2017
SHEET 16 of 150

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TITLE	BLANK		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	17 of 150

COMPRESSED IMAGE

Matira7 PCB Stackup

Foxconn stackup design

Layer NO.	Layer Name	Min. layer thickness (mil)	Typical layer thickness (mil)	Max. layer thickness (mil)	Dielectric Constant	Remark
	Solder Mask	0.40	0.50	1.80	3.70	
L1	Signal	1.40	1.90	2.40	NA	1.5 oz¡]with. Plating)
	Prepreg	2.20	2.70	3.30	3.90	
L2	Power/Gnd	1.00	1.20	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L3	Signal	1.00	1.20	1.40	NA	1 oz
	Prepreg	NA	15.00	NA	3.90	
L4	Power/Gnd	2.20	2.40	2.60	NA	2 oz
	Core	4.00	4.00	6.00	3.90	
L5	Power/Gnd	2.20	2.40	2.60	NA	2 oz
	Prepreg	NA	15.00	NA	3.90	
L6	Signal	1.00	1.20	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L7	Power/Gnd	1.00	1.20	1.40	NA	1 oz
	Prepreg	2.20	2.70	3.20	3.90	
L8	Signal	1.40	1.90	2.40	NA	1.5 oz¡]with. Plating)
	Solder Mask	0.40	0.50	1.80	3.70	
Total thickness			**61.80**			

Solder Mask	Min.	Typical	Max.
Solder Mask (a)	0.4 mil	0.7 mil	2.4 mil
Solder Mask (b, d)	0.4 mil		
Solder Mask (c)	0.4 mil	0.5 mil	1.8 mil

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COMPRESSED IMAGE

Notes :

*2: Spacing of plane 4 to plane 5 must be 4 to 6 mils

*3: Spacing of layer 3 to plane 4 must be at least 3x the distance of plane 2 to layer 3 (similarly w/ layer 6 and planes 5 & 7)

*4: Thickness spec.: 63 +/-6 mils

PCB Thickness : 63 mils

PCB Thickness Tolerance : +/- 6 mils

Impedance Calculation

Outer layer				Inner layer			
SPEC		Our design		SPEC		Our design	
Impedance target	Signal Type	Trace width/ Spacing (mil)	Simulation impedance(£[)	Impedance target	Signal Type	Trace width/ Spacing (mil)	Simulation impedance(£[)
50 ¡Ó 15%	Single-ended	4	51.33	50 ¡Ó 10%	Single-ended	5	49.9
40 ¡Ó 15%	Single-ended	6.5	40.25	40 ¡Ó 10%	Single-ended	8	39.56
85 ¡Ó 15%	Differential	5/7/5	85.17	85 ¡Ó 10%	Differential	5.3/6.2/5.3	85.3
93 ¡Ó 10%	Differential	4.5/13.5/4.5	94.42	93 ¡Ó 10%	Differential	5.1/10.3/5.1	93.32
100 ¡Ó10% (Diff.) 50¡Ó10% (Single-ended)	Differential	4.01/13.99/4.01	99.76 (Diff.) 51.27 (Single-ended)	100 ¡Ó10% (Diff.) 50¡Ó10% (Single-ended)	Differential	4.6/13/4.6	99.79 (Diff.) 51.76 (Single-ended)

PCB Stackup
Rev 0.1
May/20/2015

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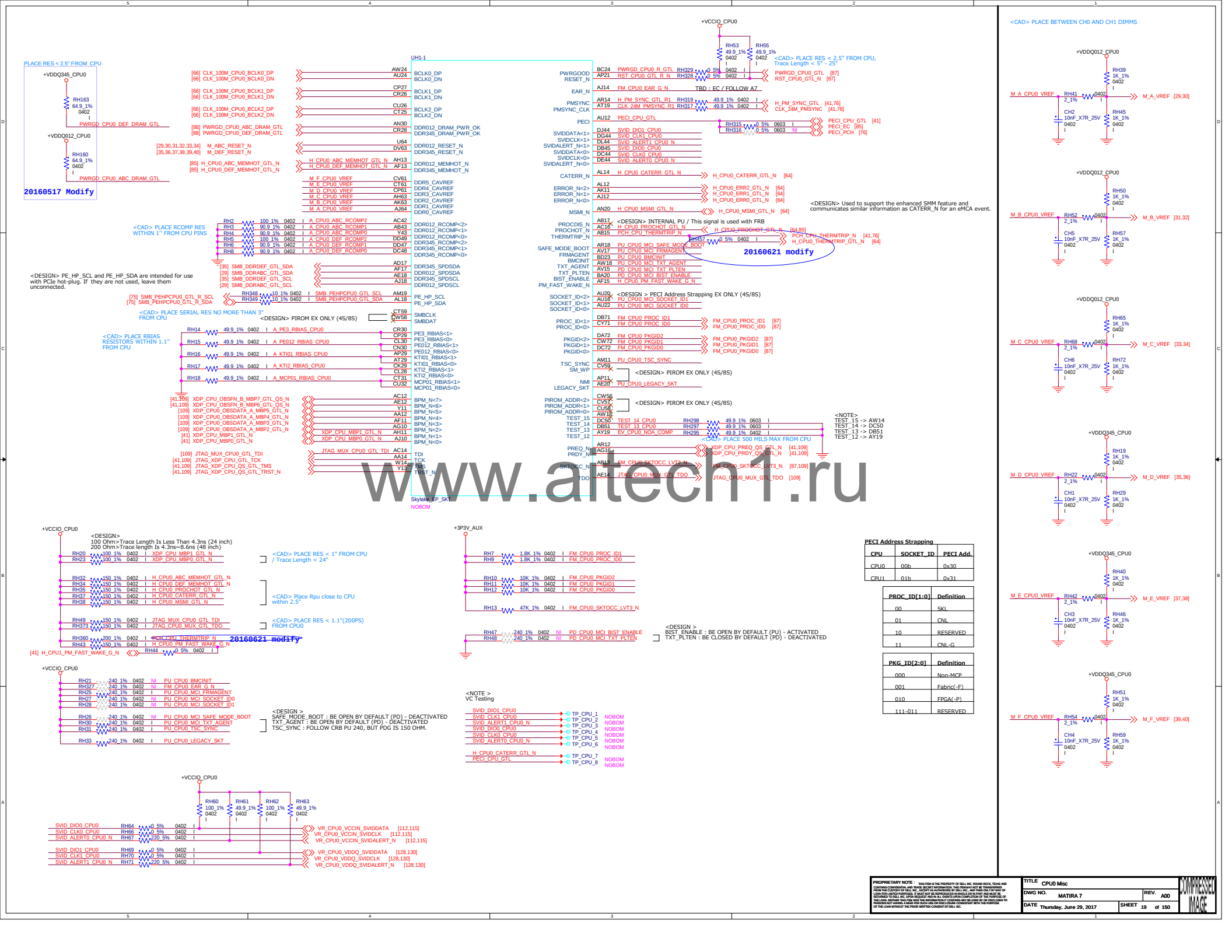
TITLE	PCB Stackup		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	18 of 150

COMPRESSED IMAGE



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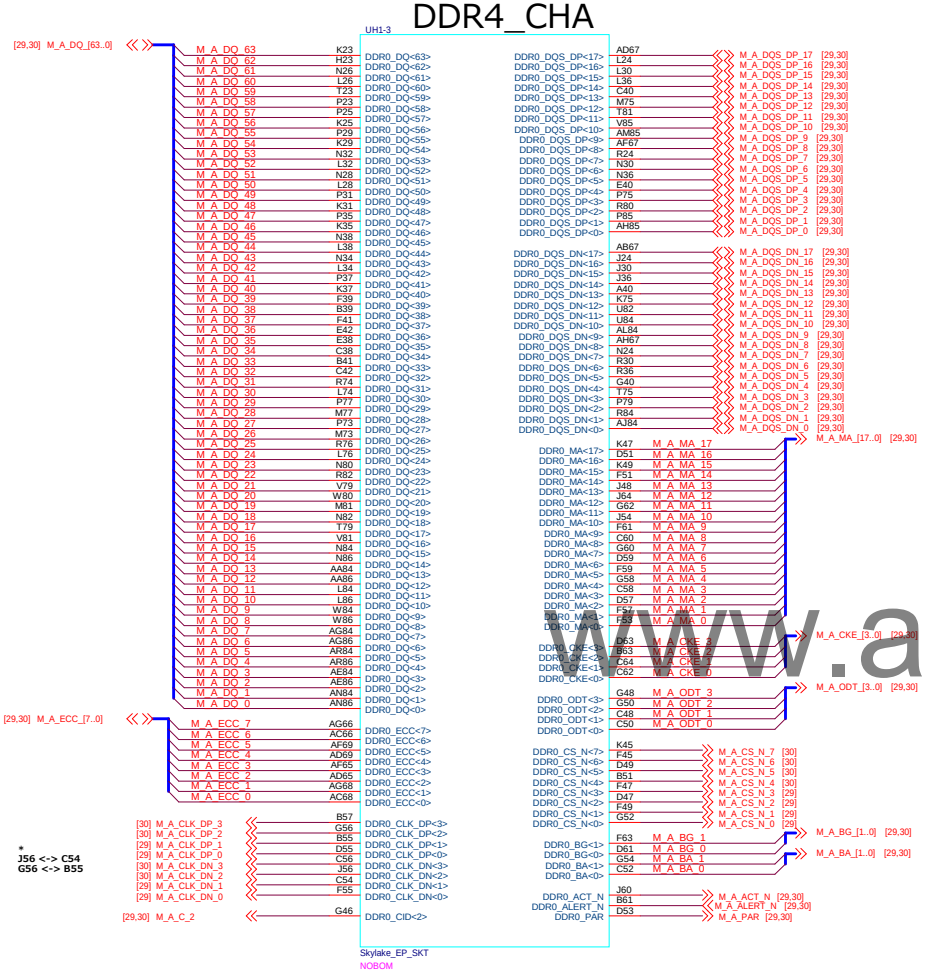
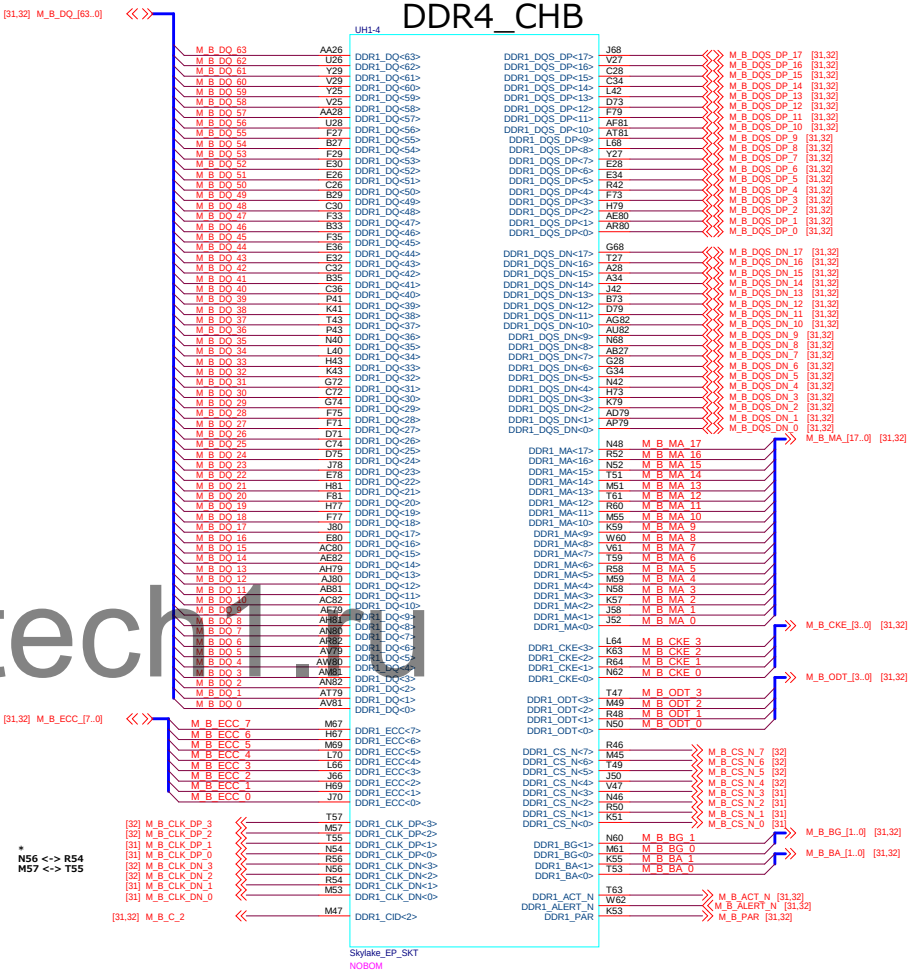
DDR4_CHA



DDR4_CHB



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TITLE	CPU0 DDR4 CHA/CHB
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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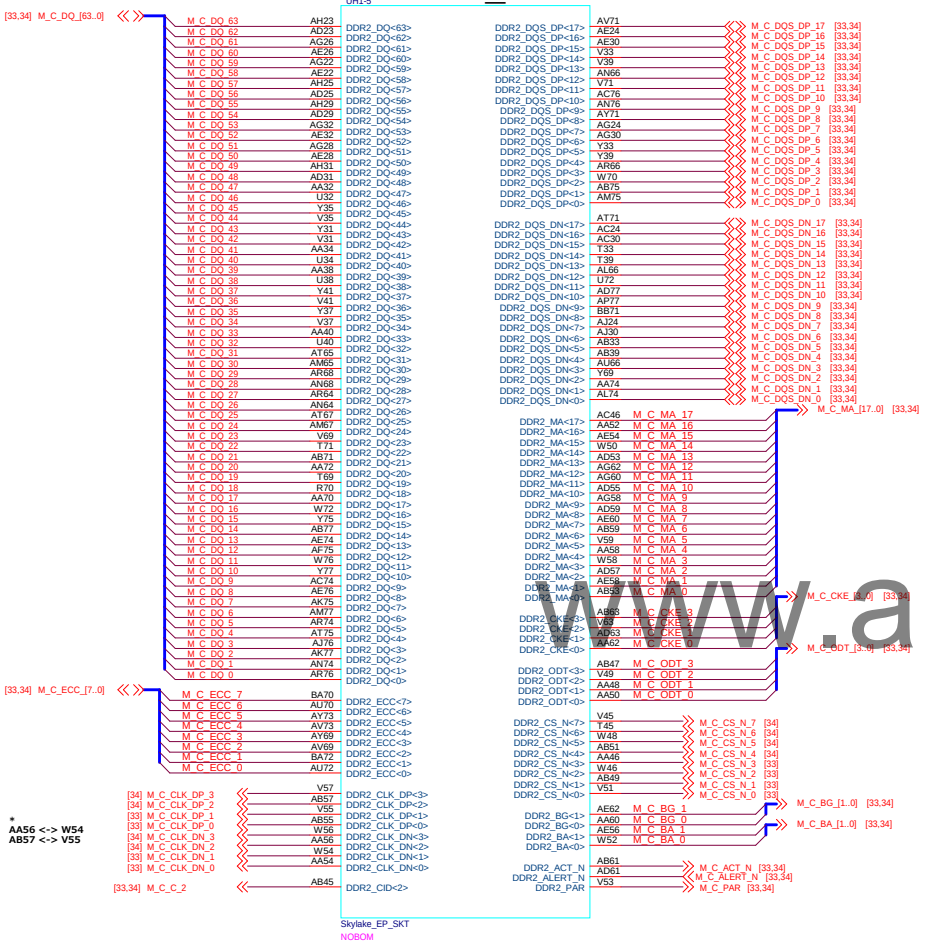
COMPRESSED IMAGE

DDR4_CHC



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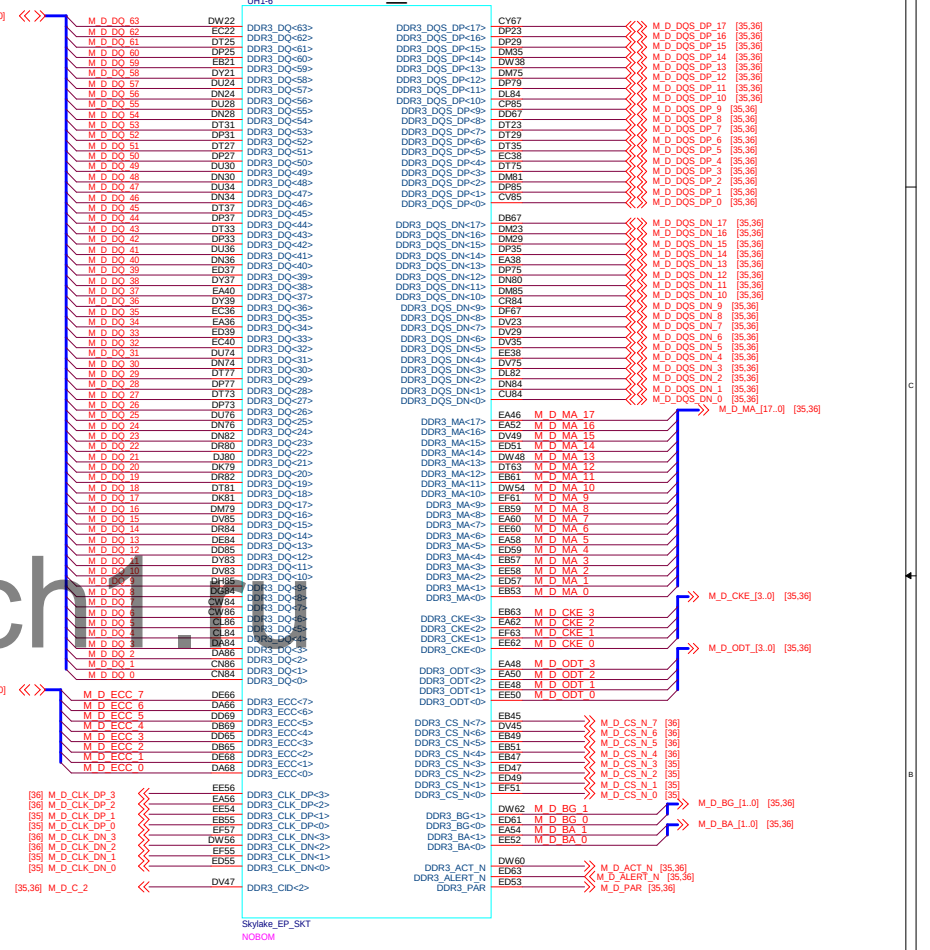

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TITLE	CPU0 DDR4 CHC/CHD
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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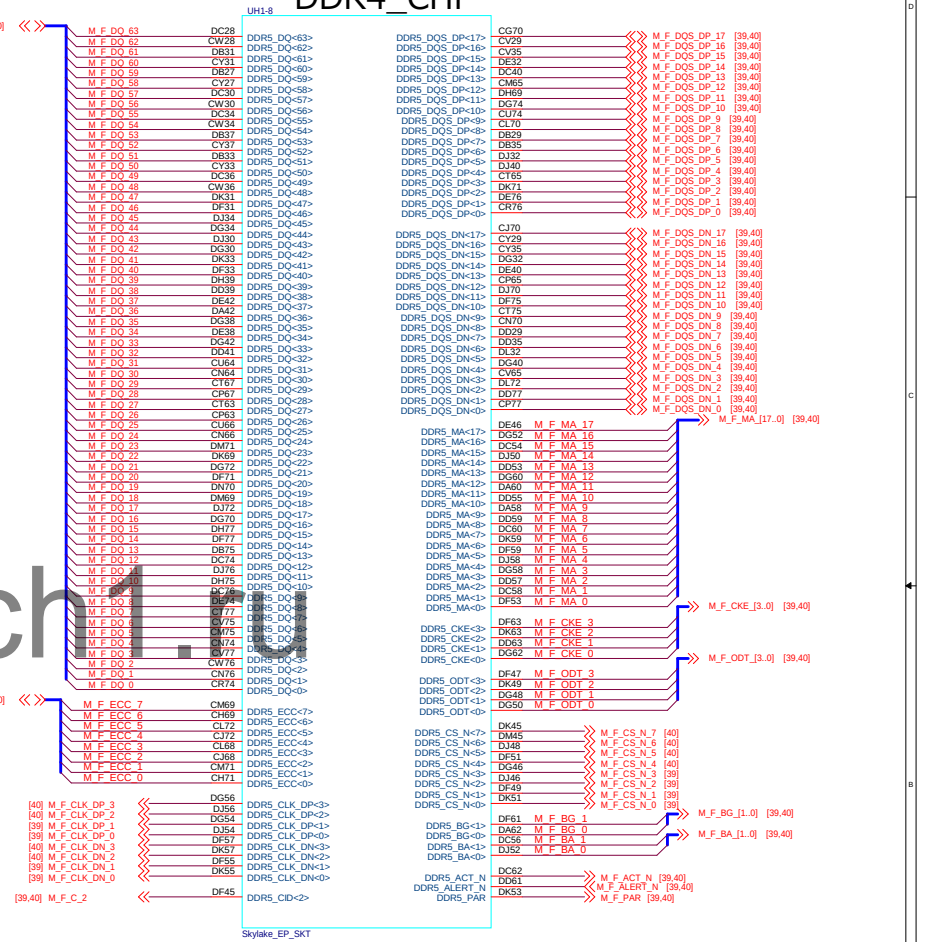
COMPRESSED IMAGE

DDR4_CHE

DDR4_CHF



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TITLE	CPU0 DDR4 CHE/CHF
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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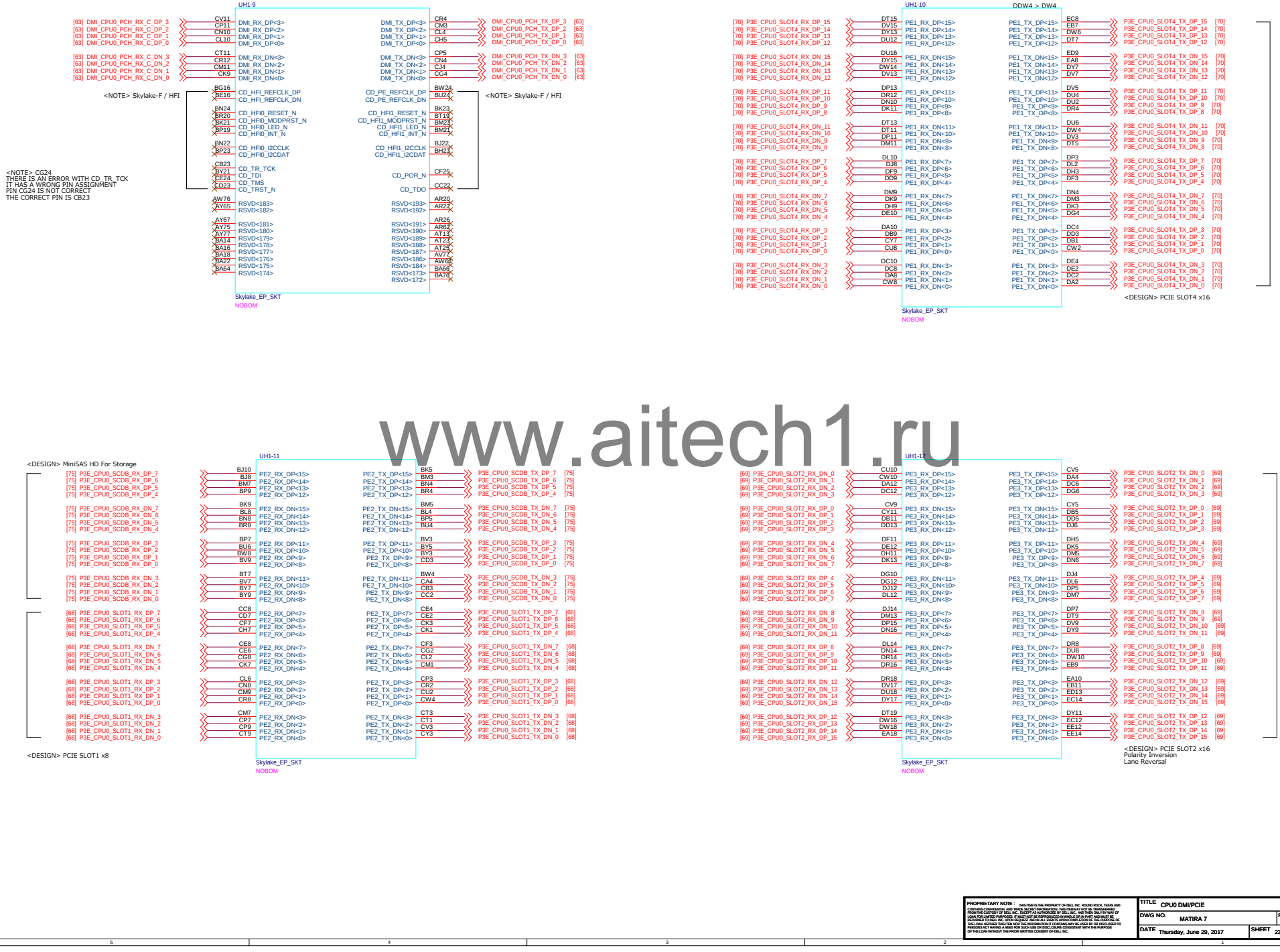
COMPRESSED IMAGE



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TITLE: CPU0 DMI/PCIE
DWG NO.: MATIRA 7
REV.: A00
DATE: Thursday, June 29, 2017
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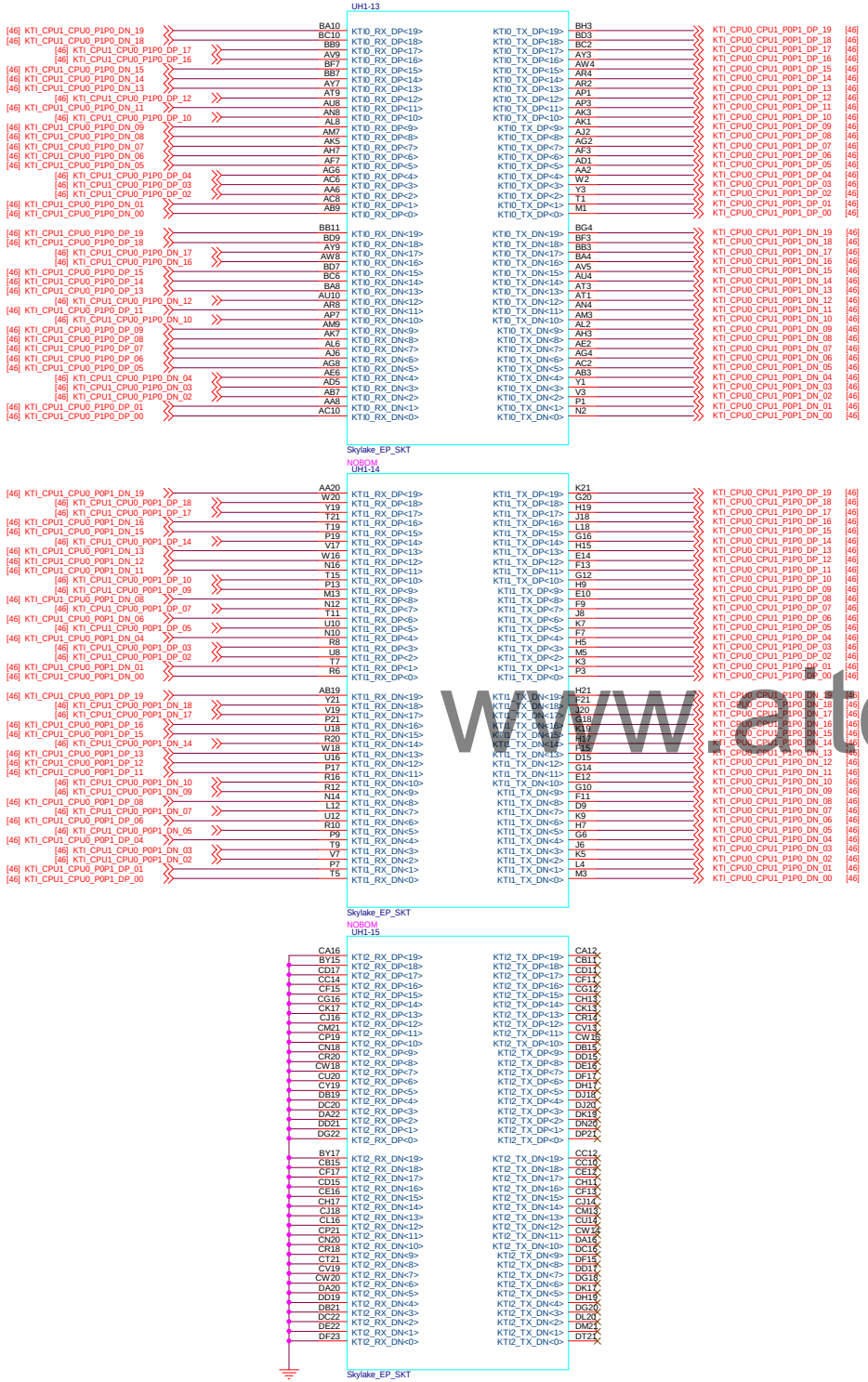
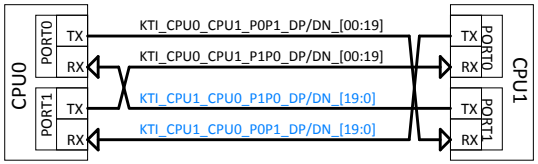
COMPRESSED IMAGE



KTI CPU0 Polarity Inversion

Lane Net Name	CPU0 Pin Name	CPU1 Pin Name	Polarity Inversion on Lane
KTI_CPU1_CPU0_P0P1_[DP/DN]_[19:00]	KTI0_RX_DP/DN[19:0]	KTI1_TX_DP/DN[19:0]	0,1,4,6,8,11,12,13,15,16,19
KTI_CPU1_CPU0_P1P0_[DP/DN]_[19:00]	KTI1_RX_DP/DN[19:0]	KTI0_TX_DP/DN[19:0]	0,1,5,6,7,8,9,11,13,14,15,18,19



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TITLE	CPU0 KTI
DWG NO.	MATIRA 7
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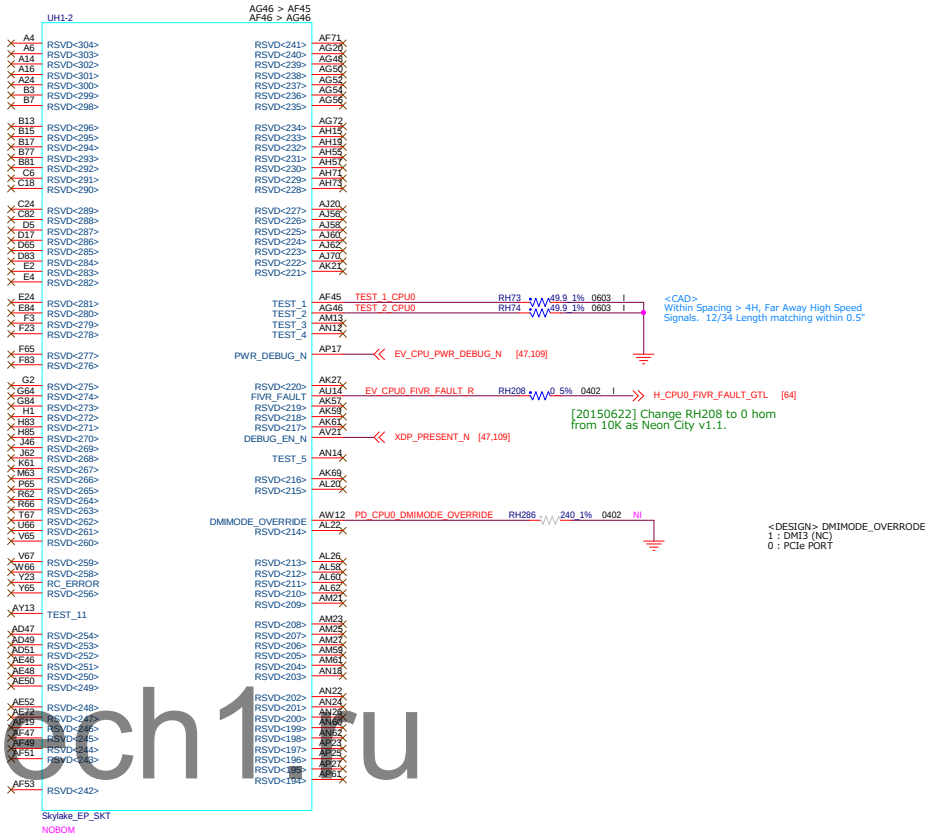
COMPRESSED IMAGE



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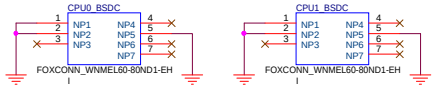
Narrow non-Fabric Bolster w/ Socket Dust Cover

xxx / H64293-001



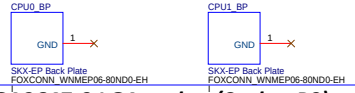
Narrow non-fabric Bolster Plate

xxx / H64294-001

Narrow Back Plate

xxx / H32155-002

20160519 modify

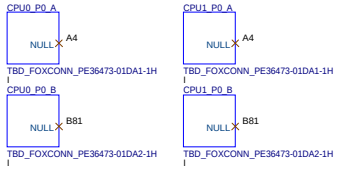


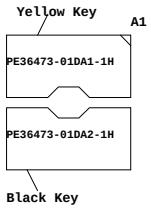
Narrow non-Fabric Package Carrier

xxx / H50071-001

LGA3647-0 LGA socket (Socket P0)

XXX / H42508-001
XXX / H42509-001





Narrow non-Fabric Socket Dust Cover

xxx / H37268-003

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TITLE	CPU0 Test/Rsvd
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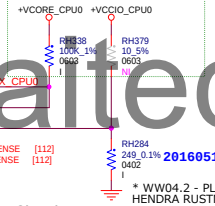
COMPRESSED IMAGE

[20150612] Cange RH338 to 100K_1% from 100ohm and add RH379 10_5%(0603) PU to VccIO to reference IBL#548692 PMAX Detection Circuit.



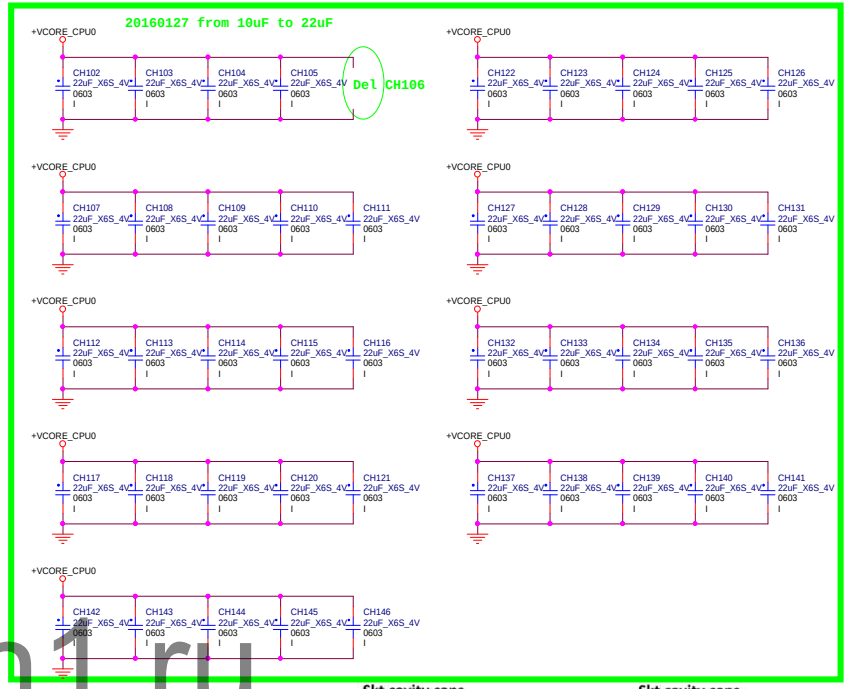
Pmax Detection Circuit

Enable	Disabled
RSense-Unstuffed (RH379)	RSense-Populate (RH379)

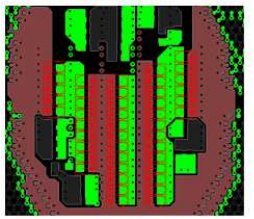
* WW04.2 - PLACE HOLDER
HENDRA RUSTMAN IS WORKING ON THIS
RES WILL BE 250 0.1%

CPU0 VccIN VR13.0 Output Caps (Top Socket Cavity)

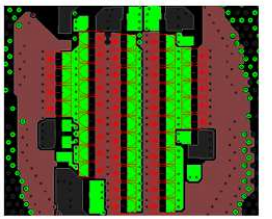
<CAD> TOP LAYER AT THE SOCKET CAVITY



Skt cavity caps
Top layer
45 x0603 10uF

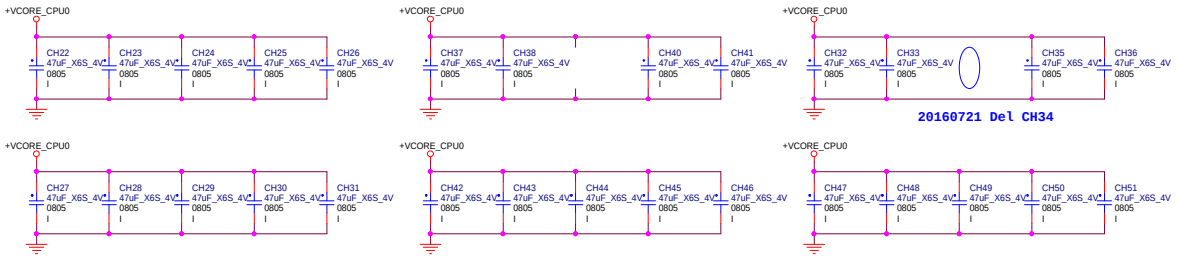


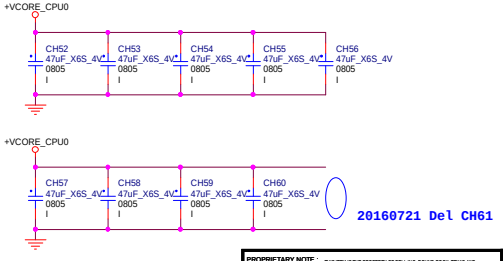
Skt cavity caps
Bot layer
40 x0805 22uF



CPU0 VccIN VR13.0 Output Caps (Bottom Socket Cavity)

<CAD> BOTTOM LAYER OF THE SOCKET CAVITY





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TITLE	CPU0 PWR-VCCIN
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COMPRESSED IMAGE

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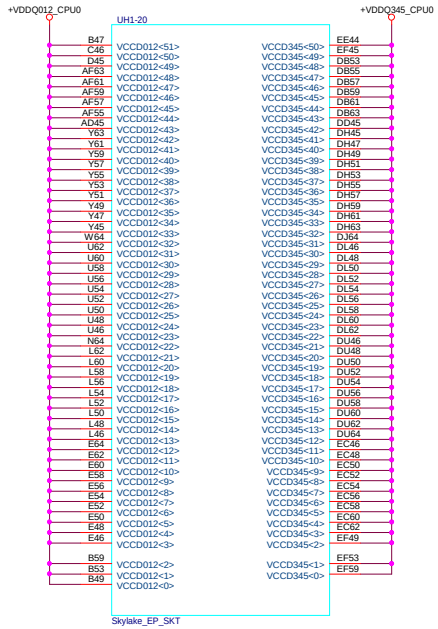
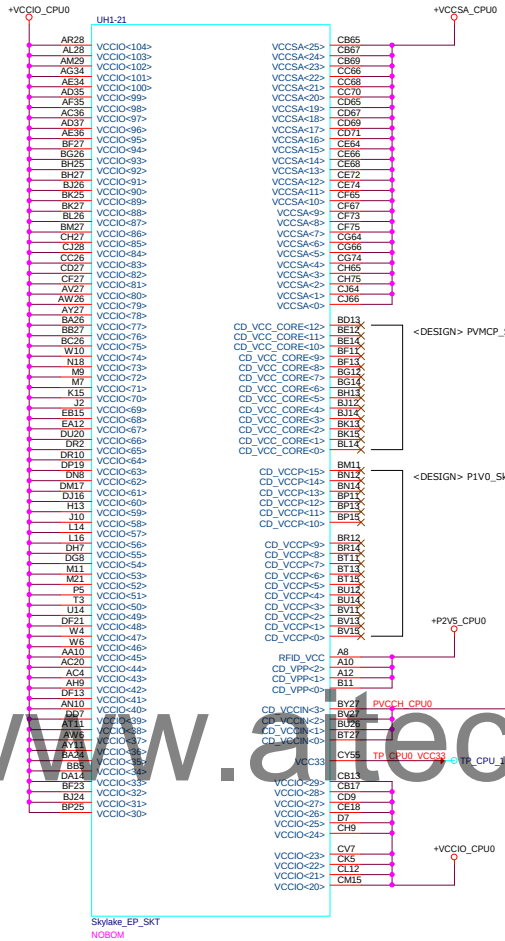
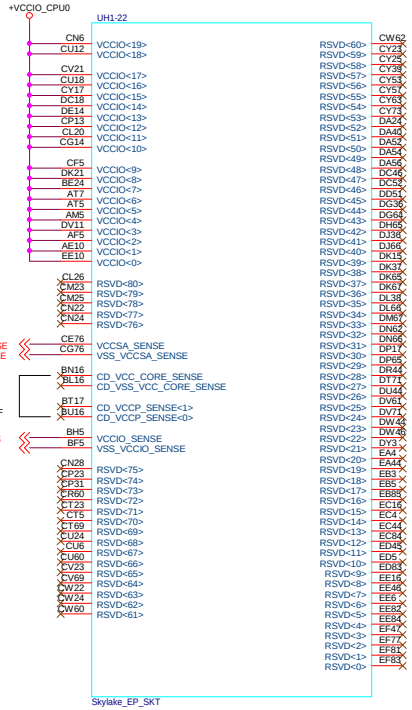
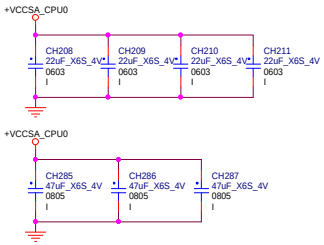






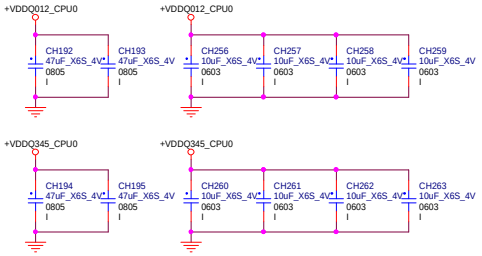
CPU0 PVCCSA VR Decoupling Caps

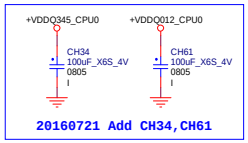
<CAD> PLACE ALL AT TOP LAYER AT SOCKET CAVITY



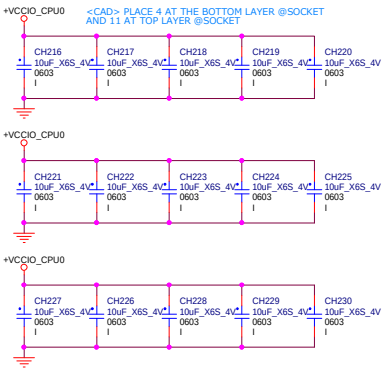
PVDDQ_ABCDEF_CPU0 VR Decoupling Caps

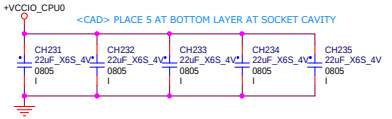
<CAD> PLACE ALL AT THE SOCKET CAVITY





CPU0 PVCCIO Decoupling Caps





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TITLE	CPU0 PWR-VCCD/VCCIO/VSA
DWG NO.	MATIRA 7
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COMPRESSED IMAGE

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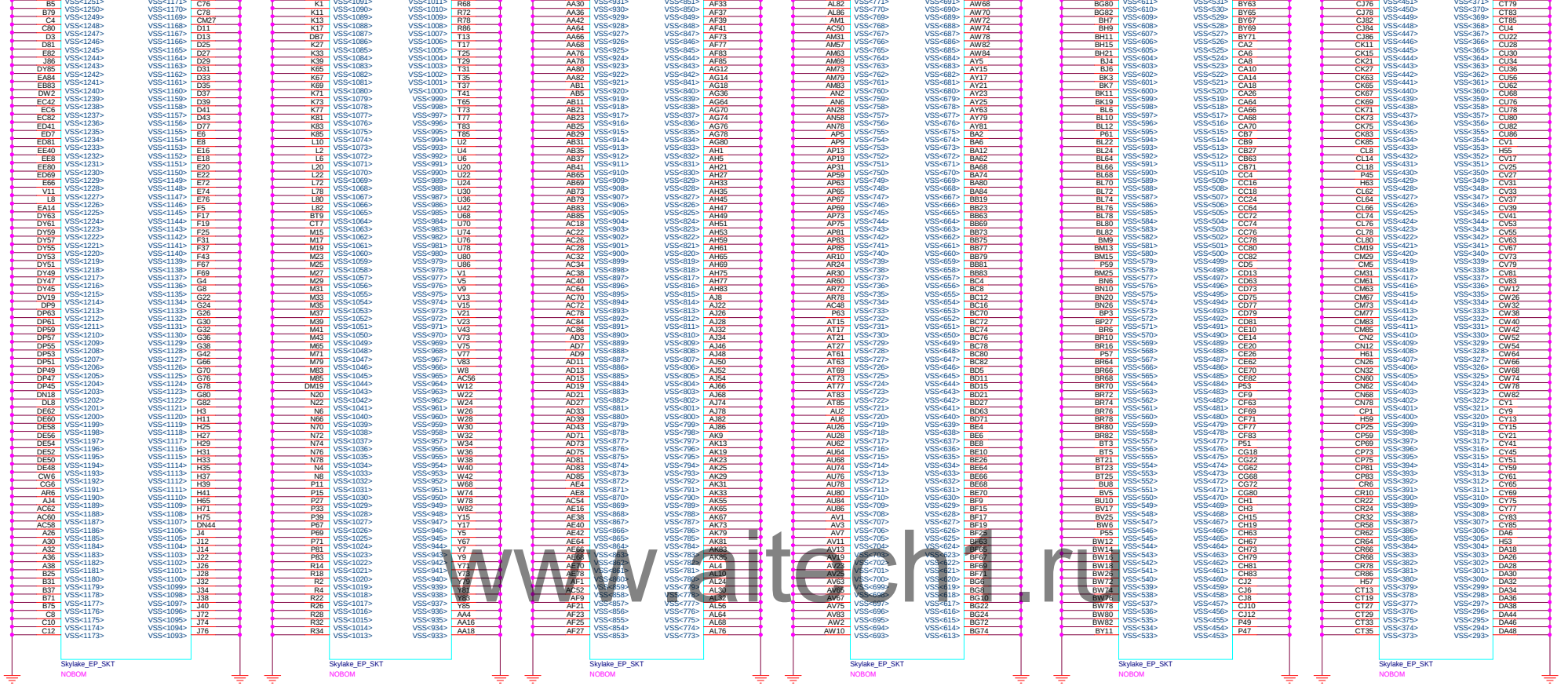

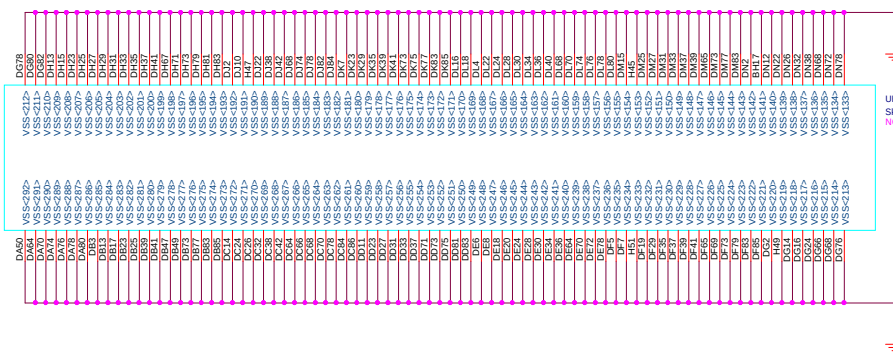

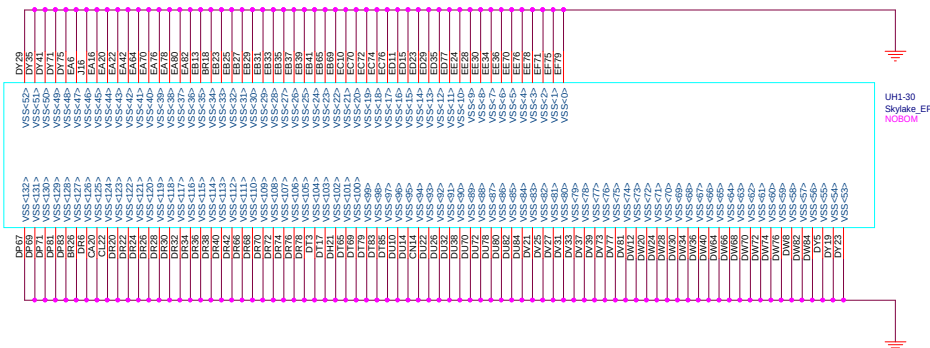

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TITLE	CPU0 Ground
DWG NO.	MATIRA 7
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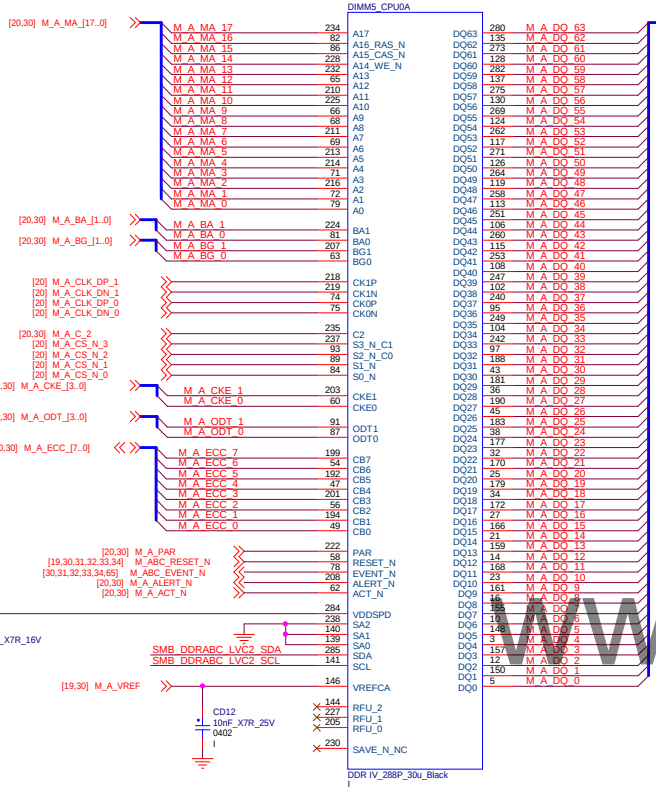
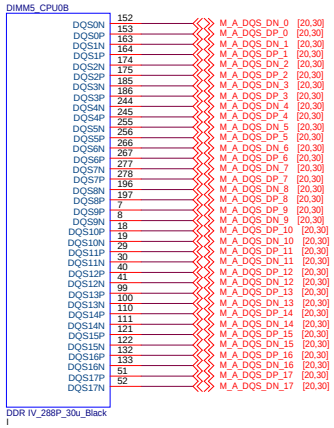
COMPRESSED IMAGE

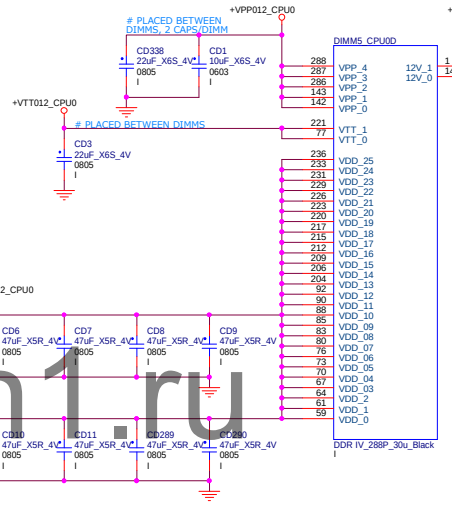
SA[2:0] = 000
SPD = 0xA0
TSOD = 0x30

DDR4 DIMM5 CPU0.CHA.D0



SPD I2C ID = A0

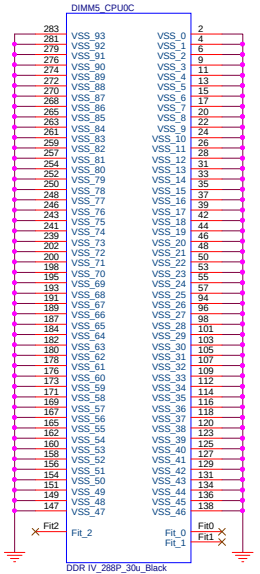




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS_AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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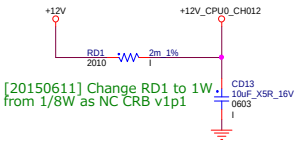
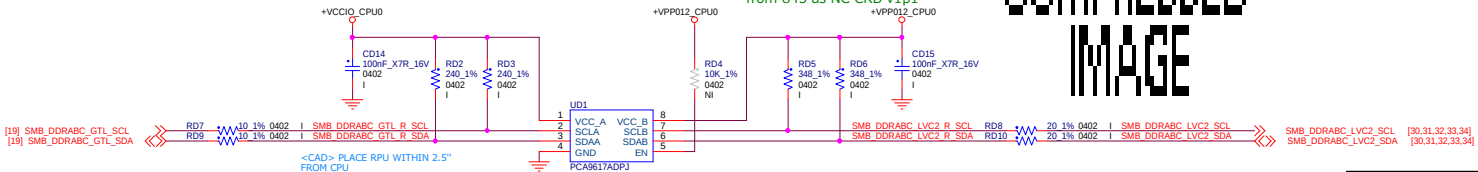
<CAD NOTE>
place close to entry of the DIMM slot at Pin#1 and Pin#145



[20150623] Change RD5/6 to 348 from 845 as NC CRB v1p1



COMPRESSED IMAGE

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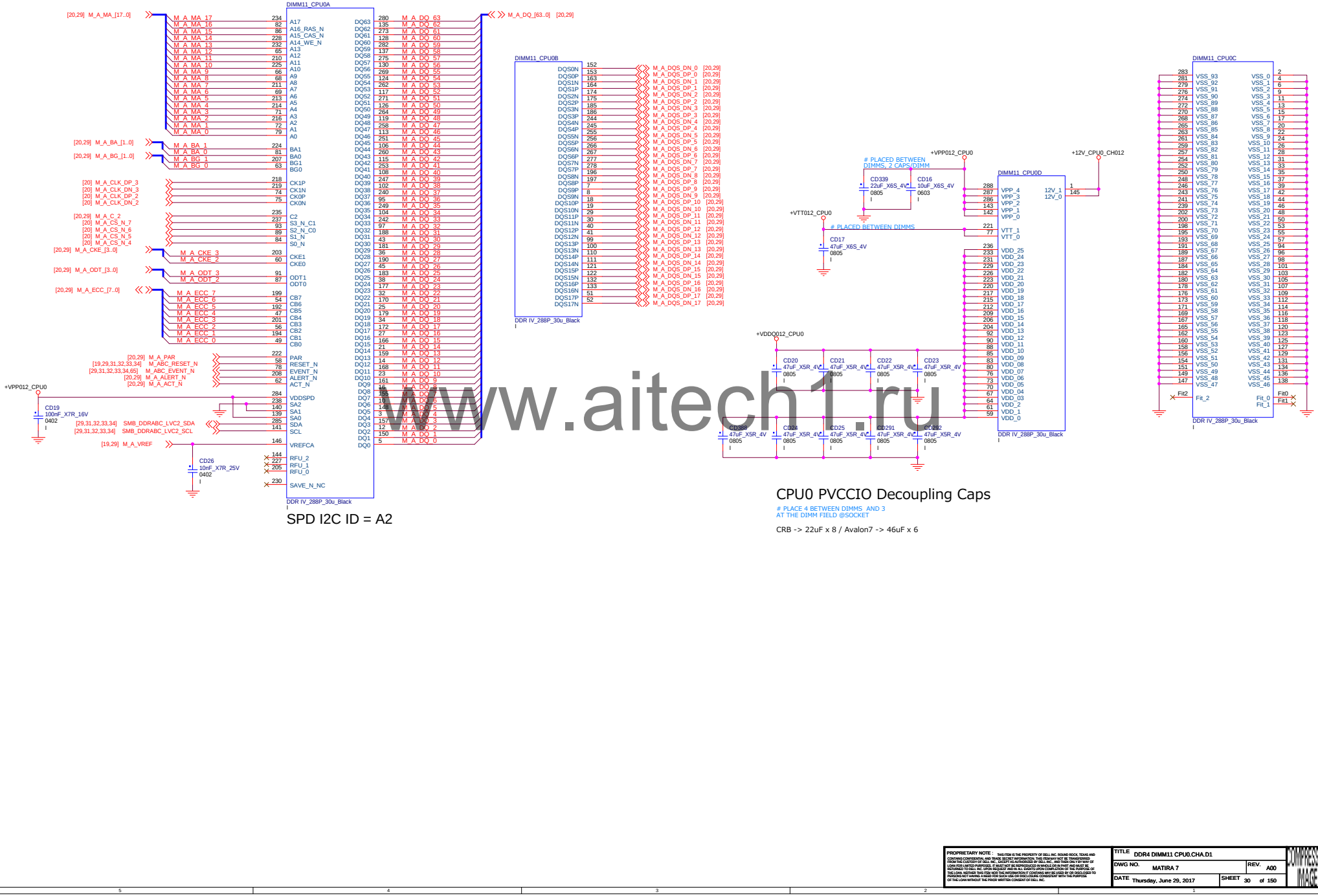
TITLE	DDR4 DIMM5 CPU0.CHA.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	29 of 150

SA[2:0] = 001
SPD = 0xA2
TSOD = 0x32

DDR4 DIMM11 CPU0.CHA.D1



SPD I2C ID = A2

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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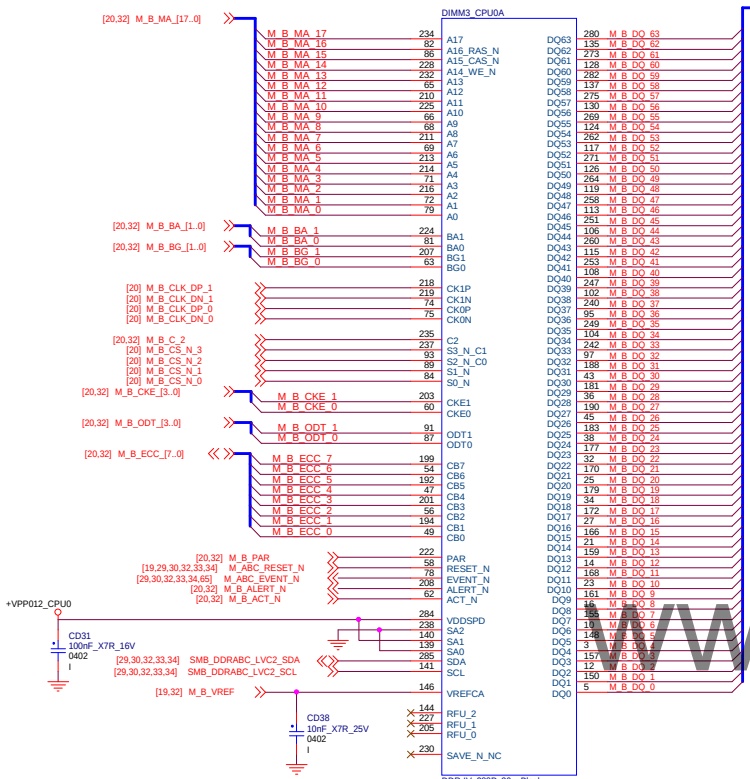
TITLE	DDR4 DIMM11 CPU0.CHA.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	30 of 150

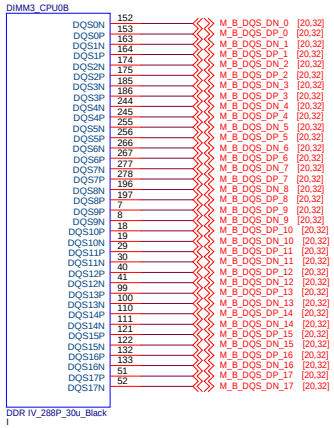
COMPRESSED IMAGE

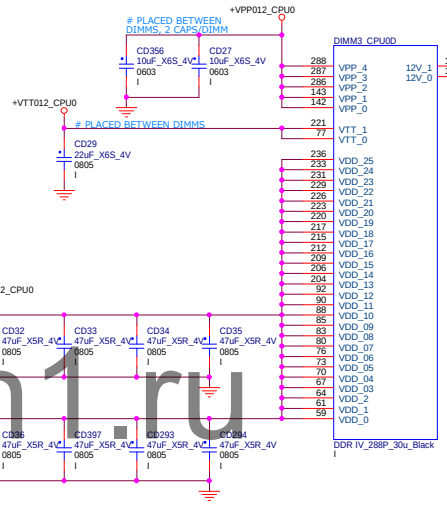
SA[2:0] = 010
SPD = 0xA4
TSOD = 0x34

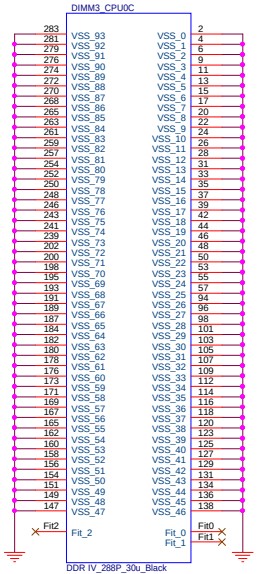
DDR4 DIMM3 CPU0.CHB.D0



SPD I2C ID = A4







CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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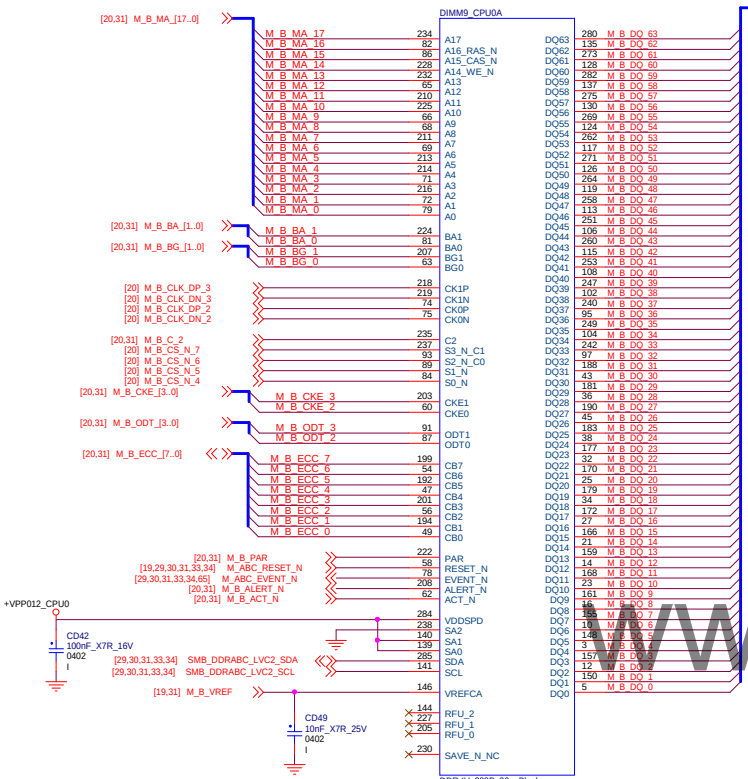
TITLE	DDR4 DIMM3 CPU0.CHB.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	31 of 150

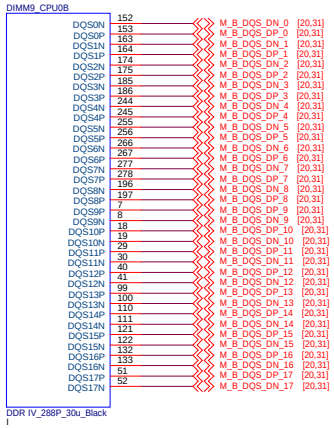
COMPRESSED IMAGE

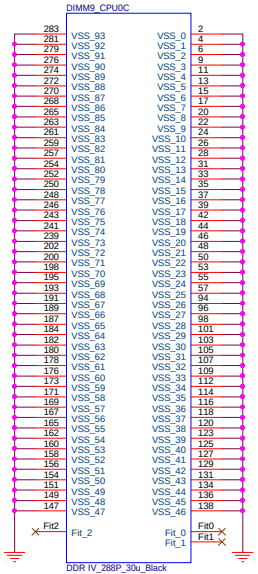
SA[2:0] = 011
SPD = 0xA6
TSOD = 0x36

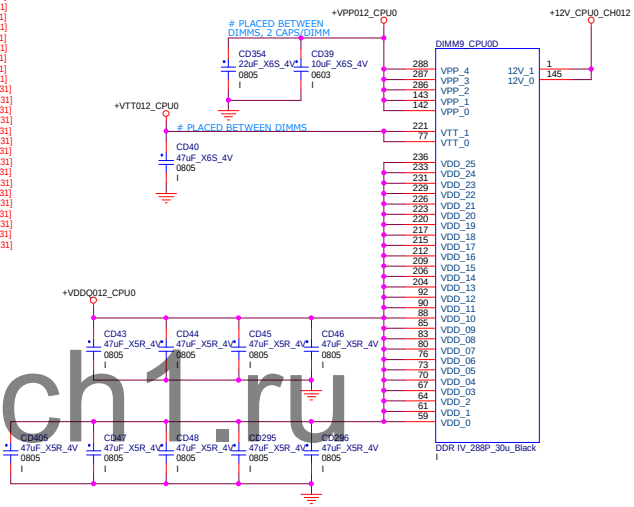
DDR4 DIMM9 CPU0.CHB.D1



SPD I2C ID = A6







CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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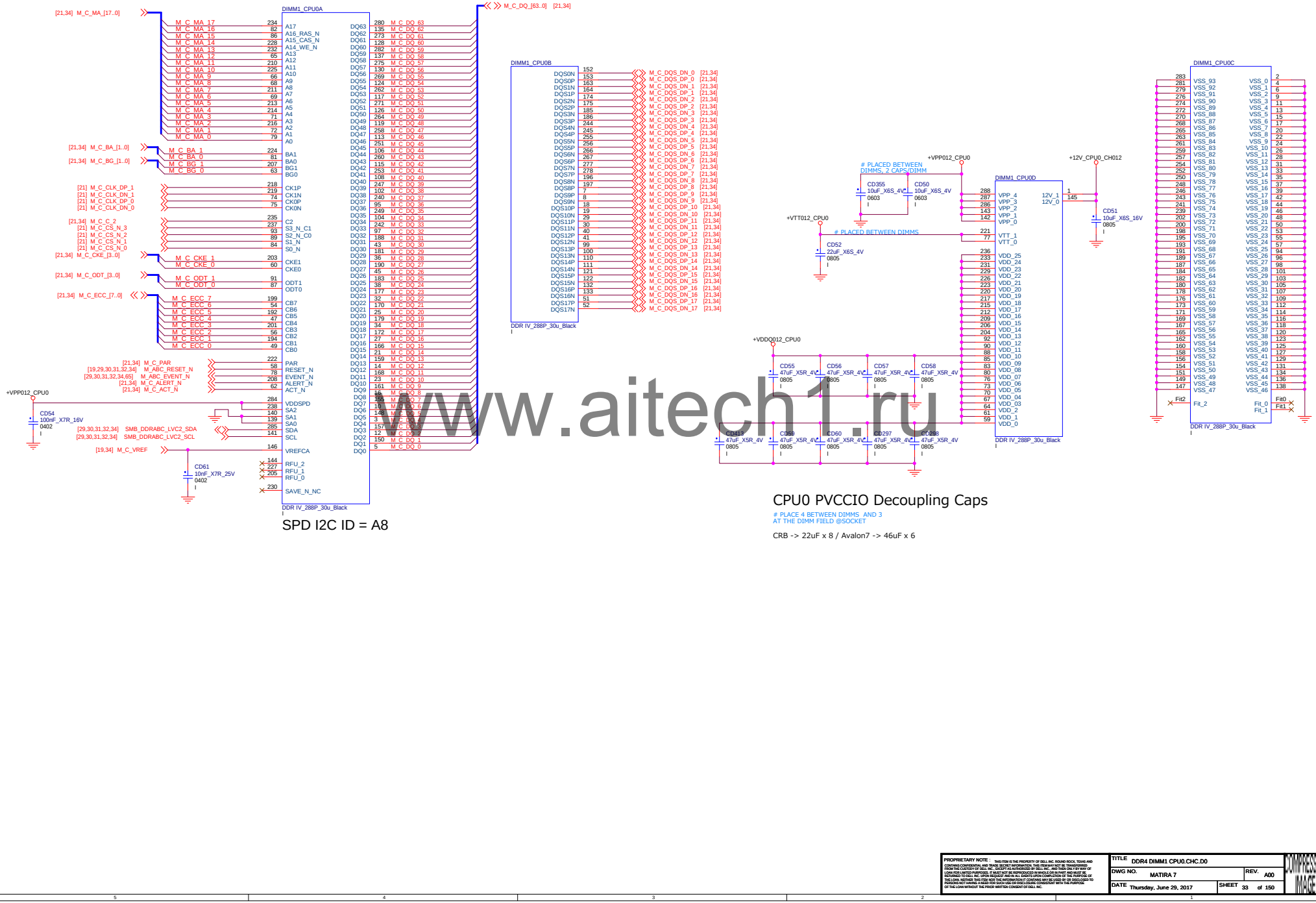
TITLE	DDR4 DIMM9 CPU0.CHB.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	32 of 150

COMPRESSED IMAGE

SA[2:0] = 100
SPD = 0xA8
TSOD = 0x38

DDR4 DIMM1 CPU0.CHC.D0



SPD I2C ID = A8

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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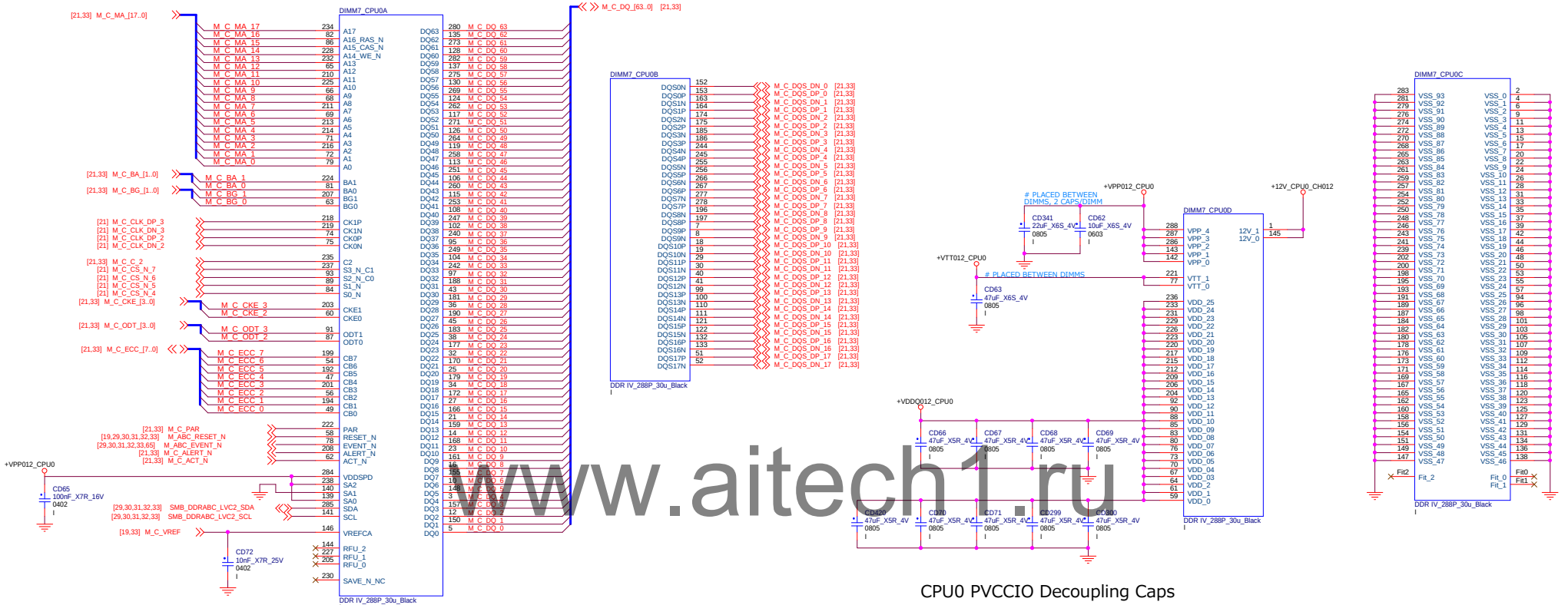
TITLE	DDR4 DIMM1 CPU0.CHC.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	33 of 150

COMPRESSED IMAGE

SA[2:0] = 101
SPD = 0xAA
TSOD = 0x3A

DDR4 DIMM7 CPU0.CHC.D1



SPD I2C ID = AA

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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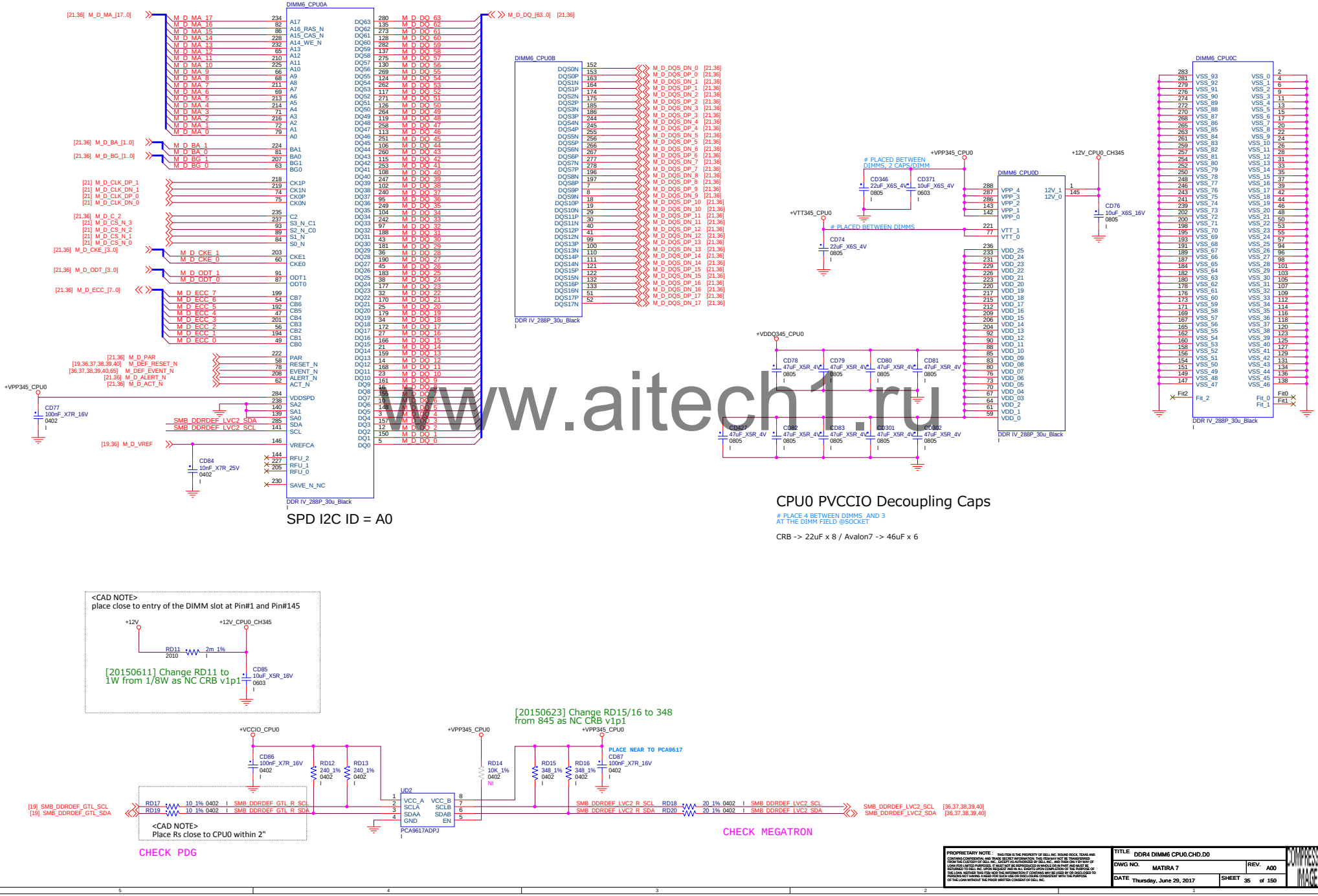
TITLE	DDR4 DIMM7 CPU0.CHC.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	34 of 150

COMPRESSED IMAGE

SA[2:0] = 000
SPD = 0xA0
TSOD = 0x30

DDR4 DIMM6 CPU0.CHD.D0



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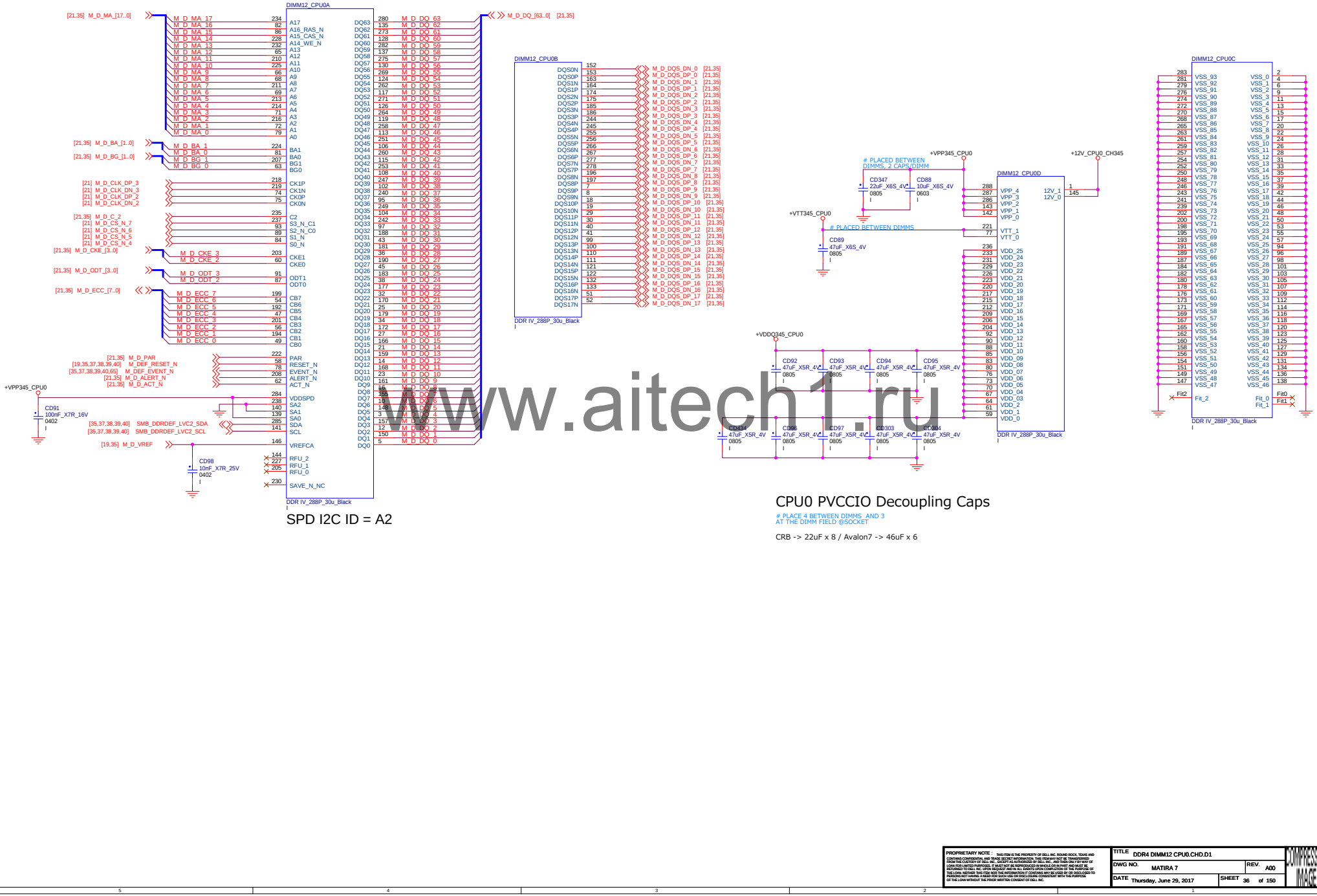
TITLE	DDR4 DIMM6 CPU0.CHD.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	35 of 150

COMPRESSED IMAGE

SA[2:0] = 001
SPD = 0xA2
TSOD = 0x32

DDR4 DIMM12 CPU0.CHD.D1



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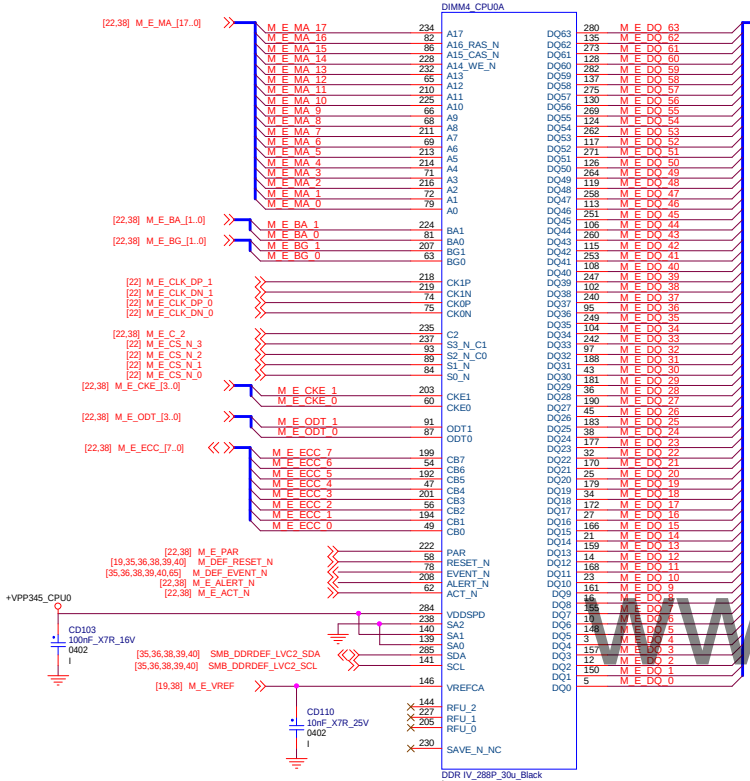
TITLE	DDR4 DIMM12 CPU0.CHD.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	36 of 150

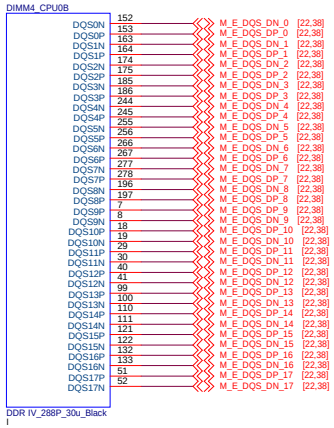
COMPRESSED IMAGE

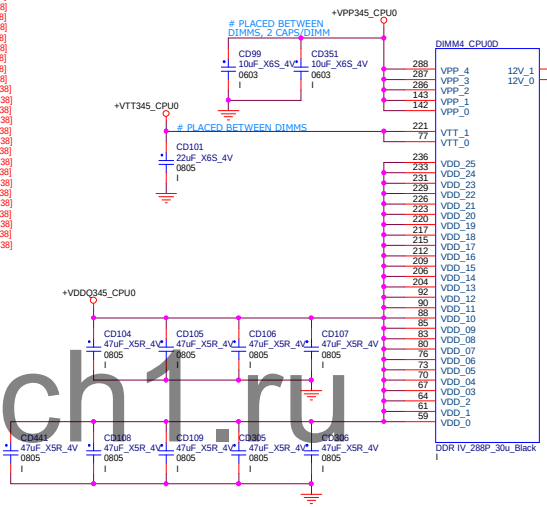
SA[2:0] = 010
SPD = 0xA4
TSOD = 0x34

DDR4 DIMM4 CPU0.CHE.D0



SPD I2C ID = A4

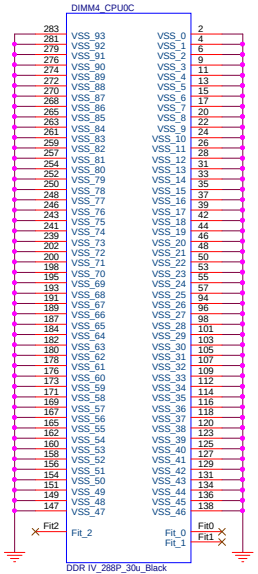




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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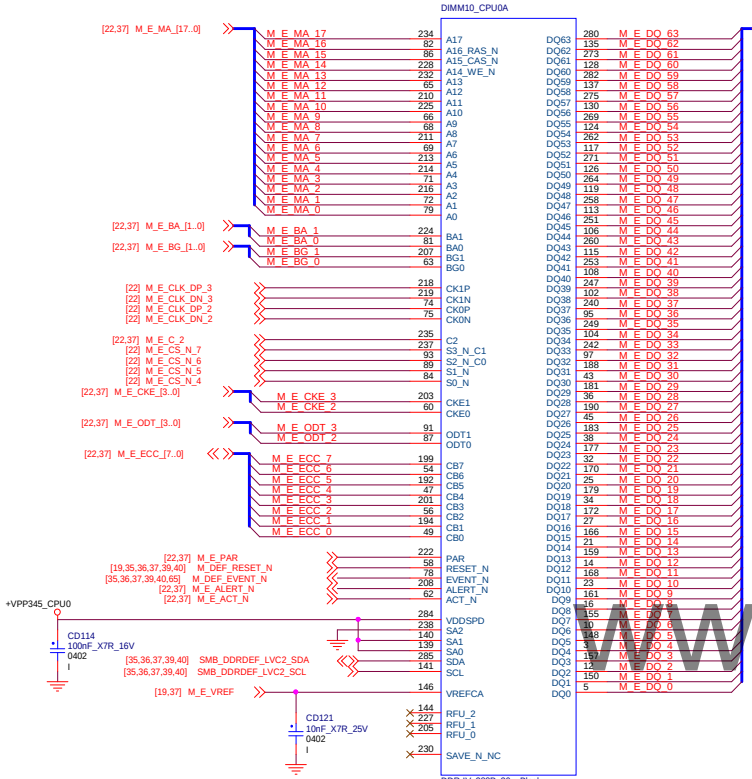
TITLE: DDR4 DIMM4 CPU0.CHE.D0
DWG NO.: MATIRA 7
REV.: A00
DATE: Thursday, June 29, 2017
SHEET: 37 of 150

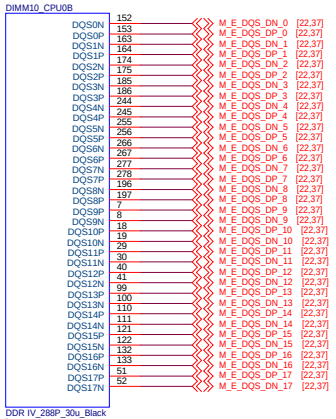
COMPRESSED IMAGE

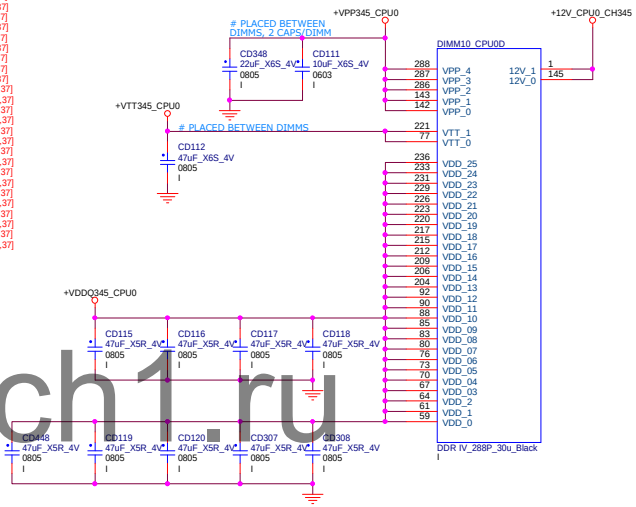
SA[2:0] = 011
SPD = 0xA6
TSOD = 0x36

DDR4 DIMM10 CPU0.CHE.D1



SPD I2C ID = A6

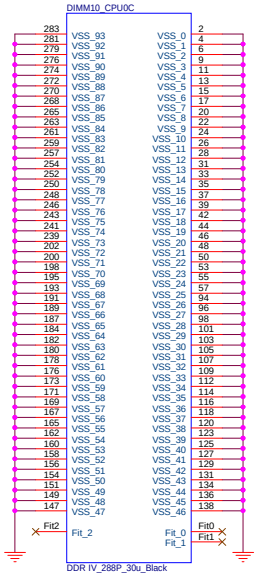




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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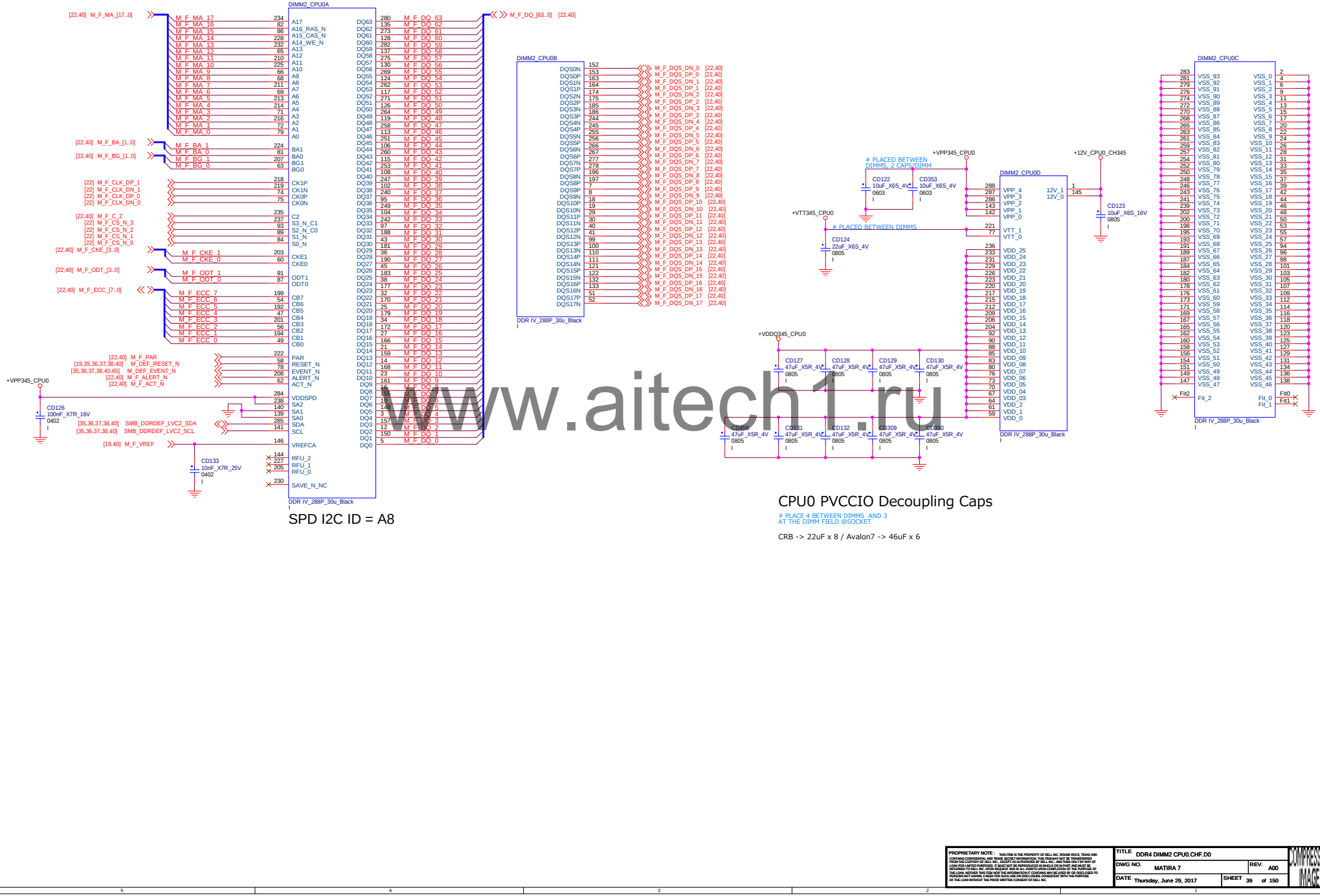
TITLE	DDR4 DIMM10 CPU0.CHE.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	38 of 150

UNCOMPRESSED IMAGE

SA[2:0] = 100
SPD = 0xA8
TSOD = 0x38

DDR4 DIMM2 CPU0.CHF.D0



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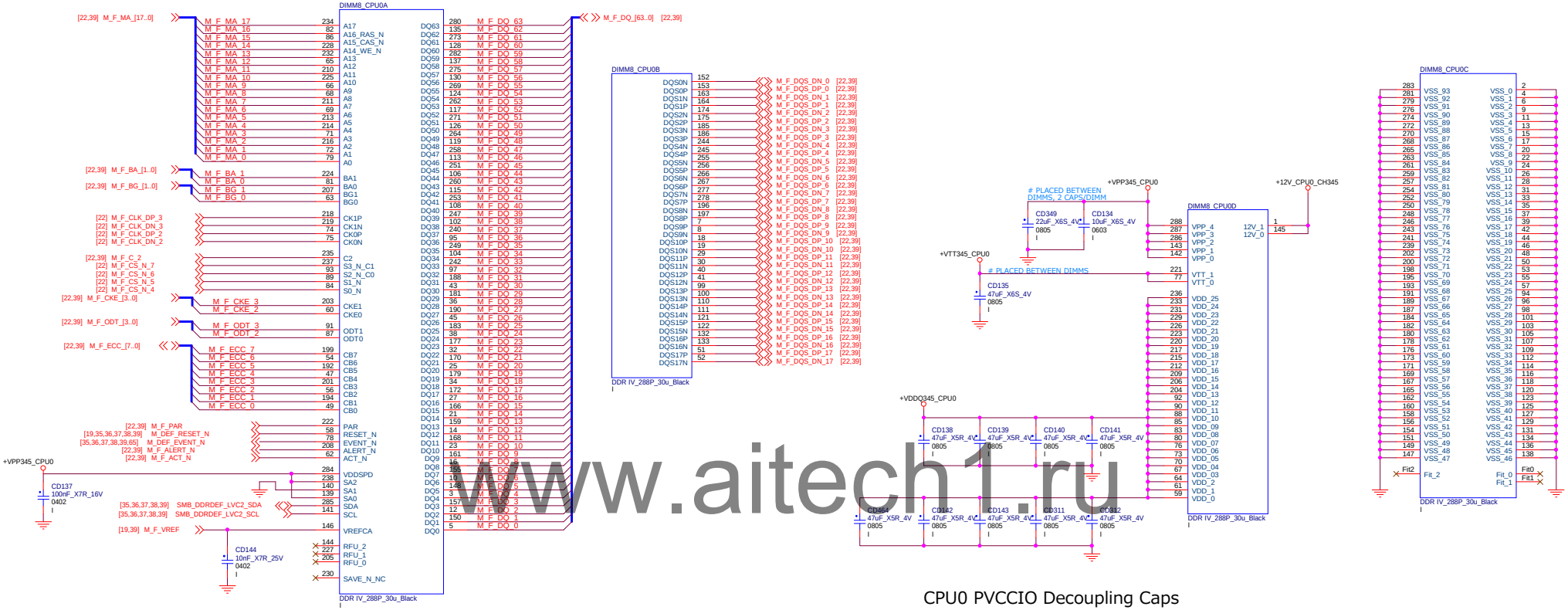
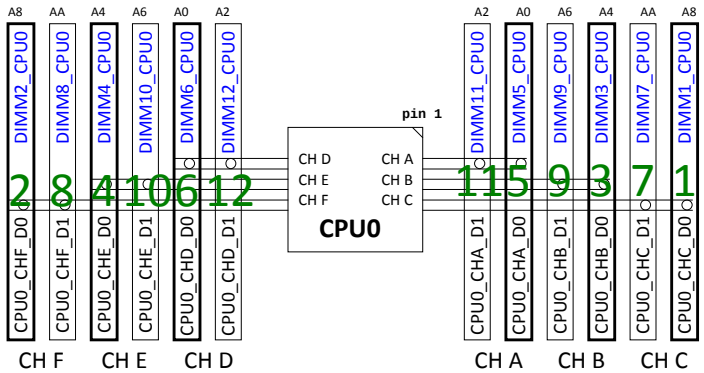
TITLE	DDR4 DIMM2 CPU0.CHF.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	39 of 150

COMPRESSED IMAGE

SA[2:0] = 101
SPD = 0xAA
TSOD = 0x3A

DDR4 DIMM8 CPU0.CHF.D1





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TITLE	DDR4 DIMM8 CPU0.CHF.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	40 of 150

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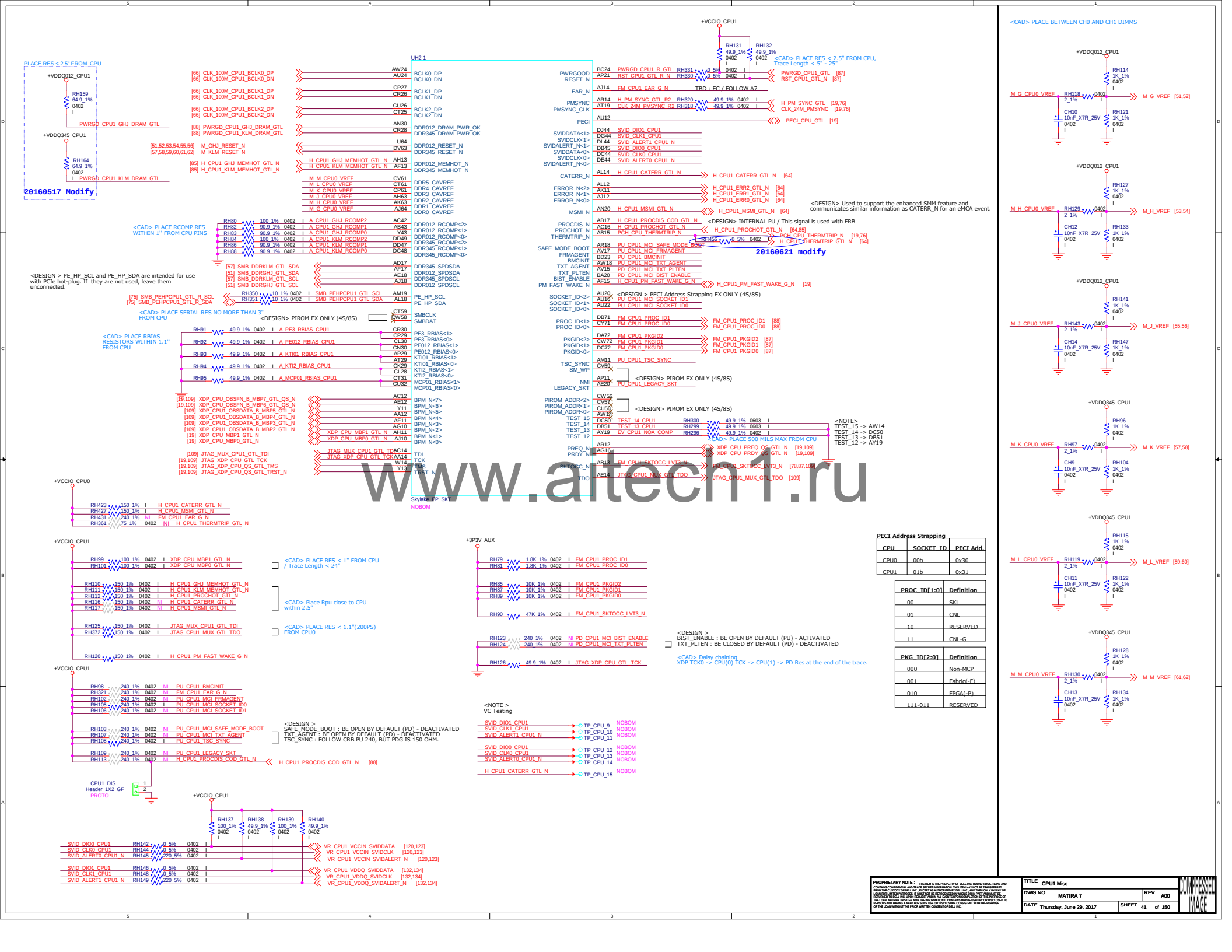
COMPRESSED IMAGE



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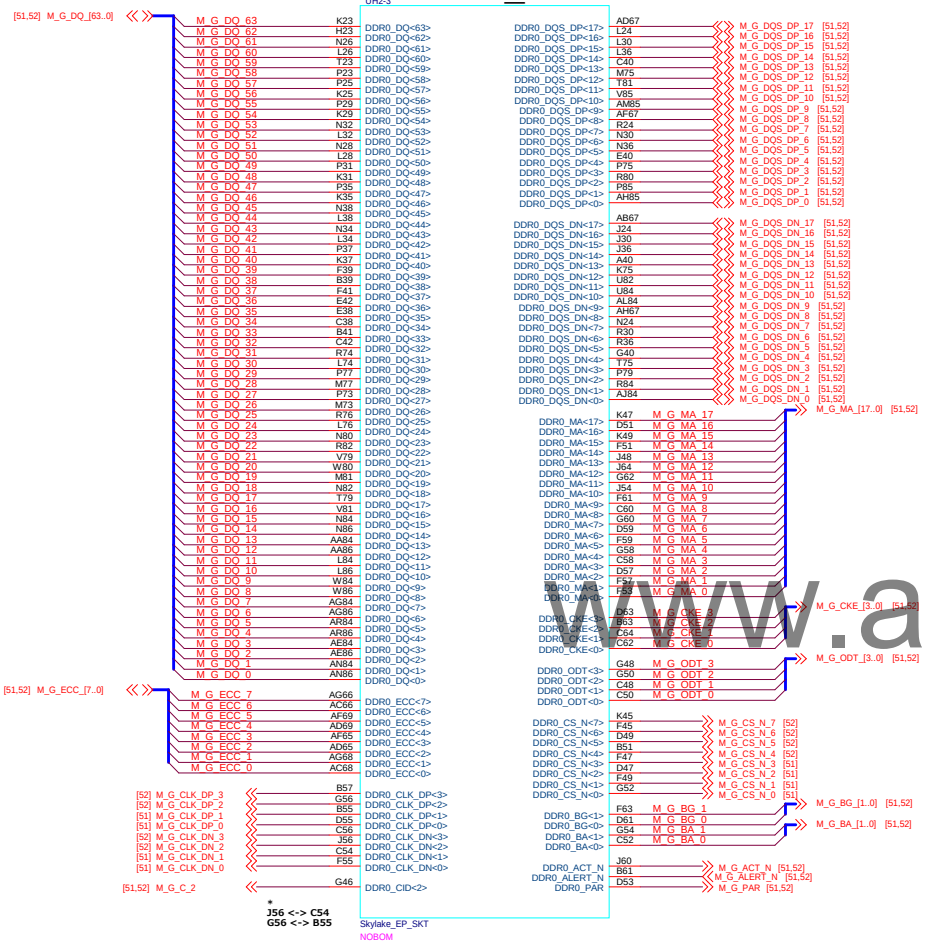
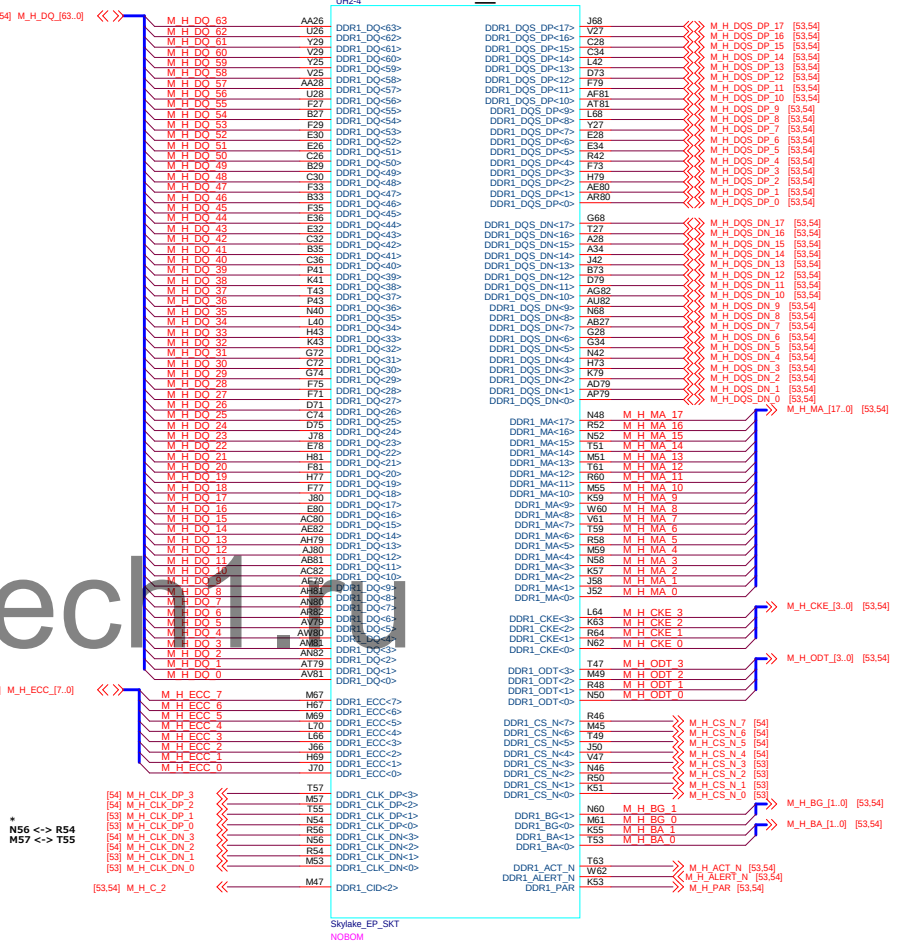
DDR4_CHG



DDR4_CHH



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TITLE	CPU1 DDR4 CHG/CHH
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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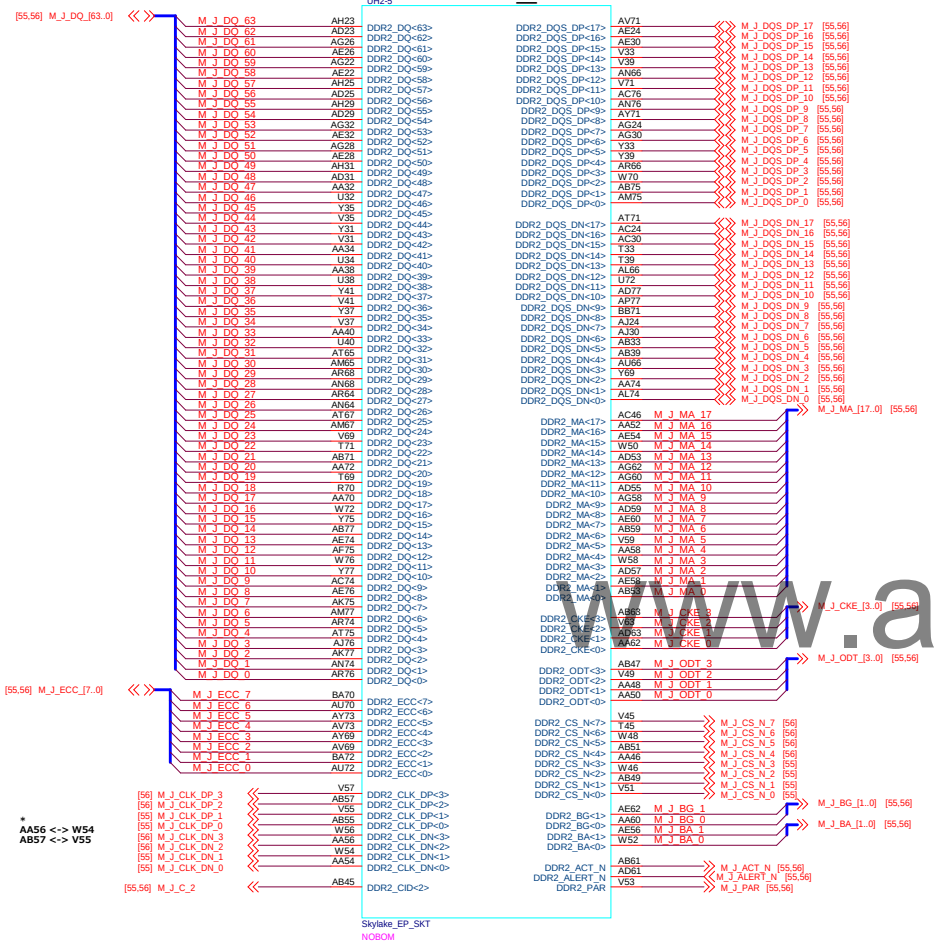
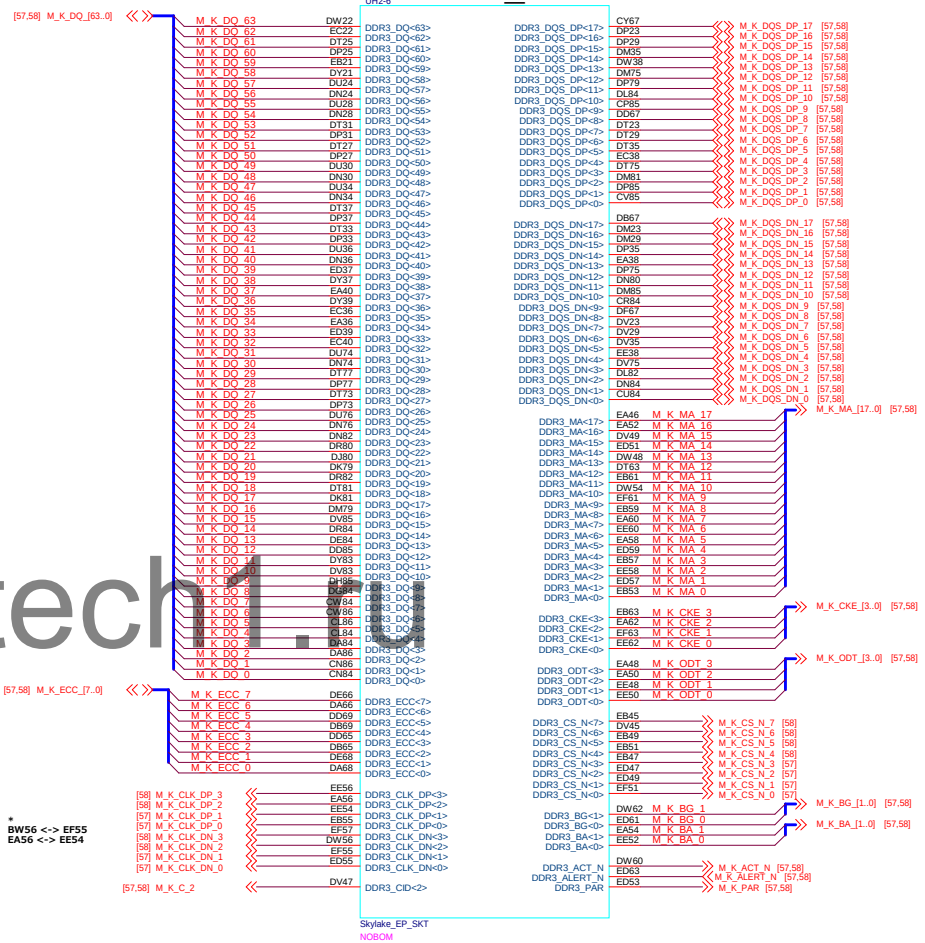
COMPRESSED IMAGE

DDR4_CHJ



DDR4_CHK



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TITLE	CPU1 DDR4 CHJ/CHK
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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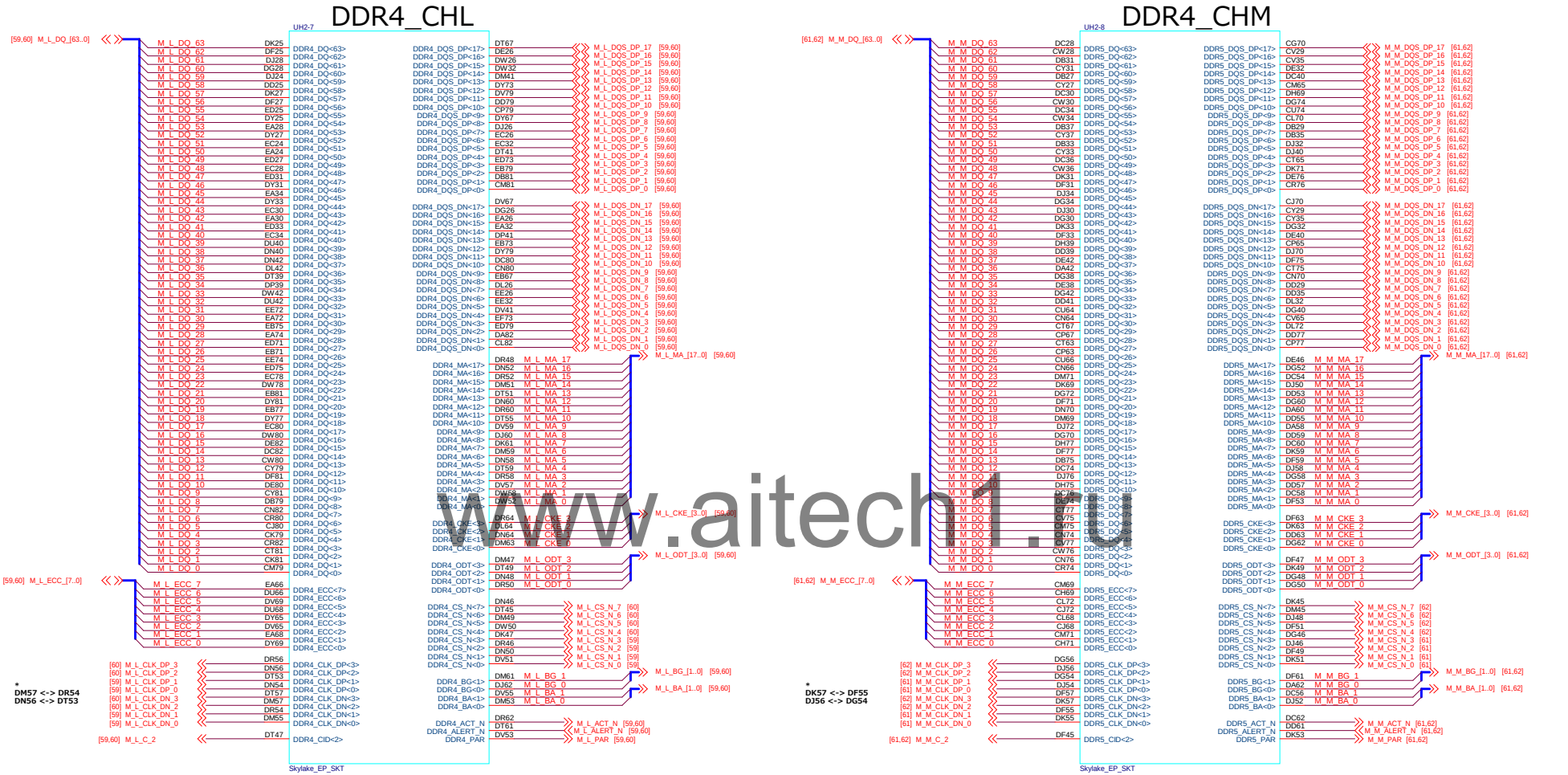
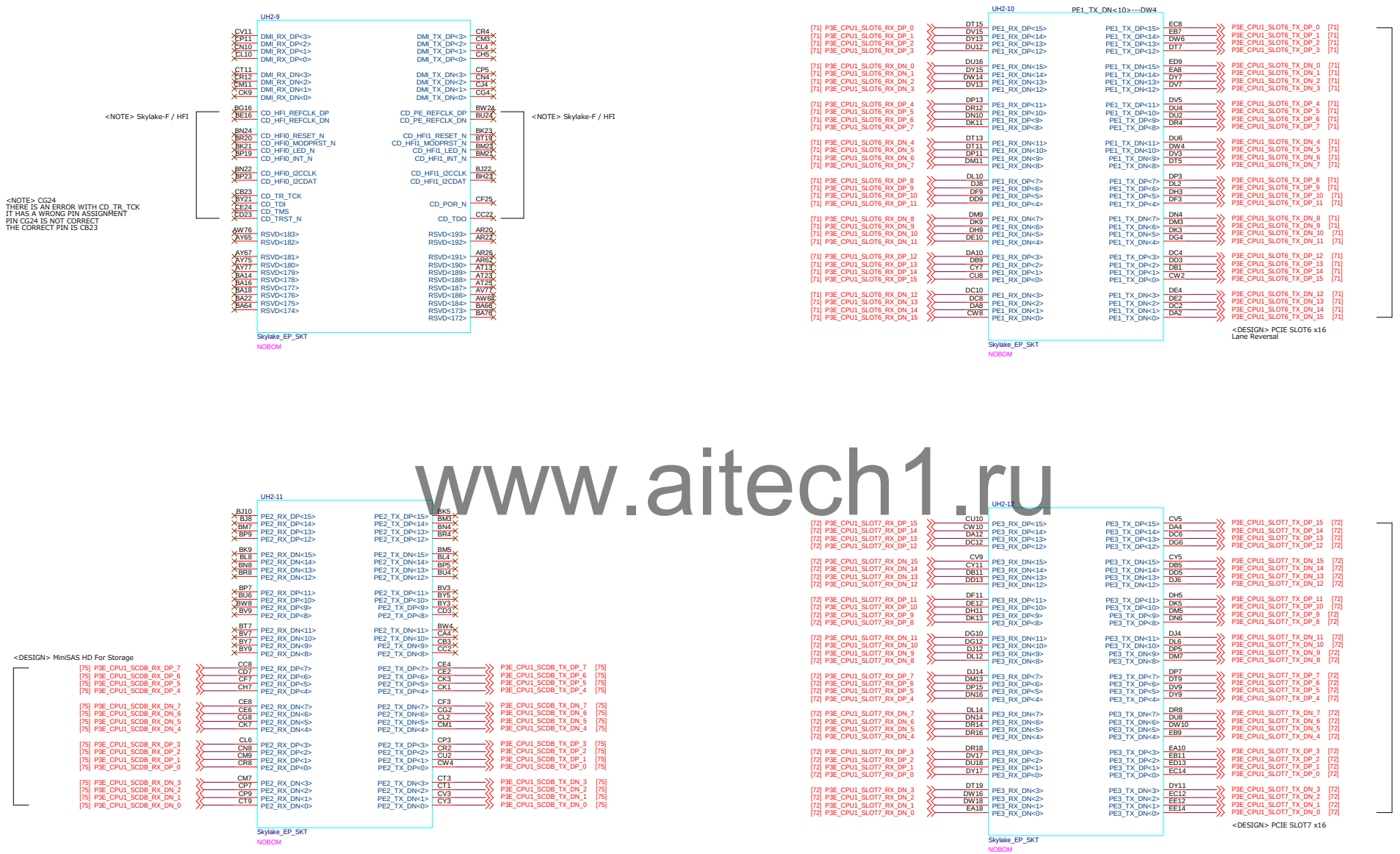
COMPRESSED IMAGE



www.aitech.ir



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TITLE	CPU1 DMI/PCIE
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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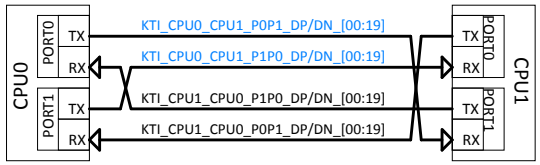
COMPRESSED IMAGE

KTI CPU1 Polarity Inversion

Lane Net Name	CPU0 Pin Name	CPU1 Pin Name	Polarity Inversion on Lane
KTI_CPU0_CPU1_P0P1_DP/DN_[00:19]	KTI0_TX_DP/DN[19:0]	KTI1_RX_DP/DN[19:0]	0,1,4,6,8,11,12,13,15,16,19
KTI_CPU0_CPU1_P1P0_DP/DN_[00:19]	KTI1_TX_DP/DN[19:0]	KTI0_RX_DP/DN[19:0]	0,1,5,6,7,8,9,11,13,14,15,18,19



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TITLE CPU1 KTI

DWG NO. MATIRA 7

REV. A00

DATE Thursday, June 29, 2017

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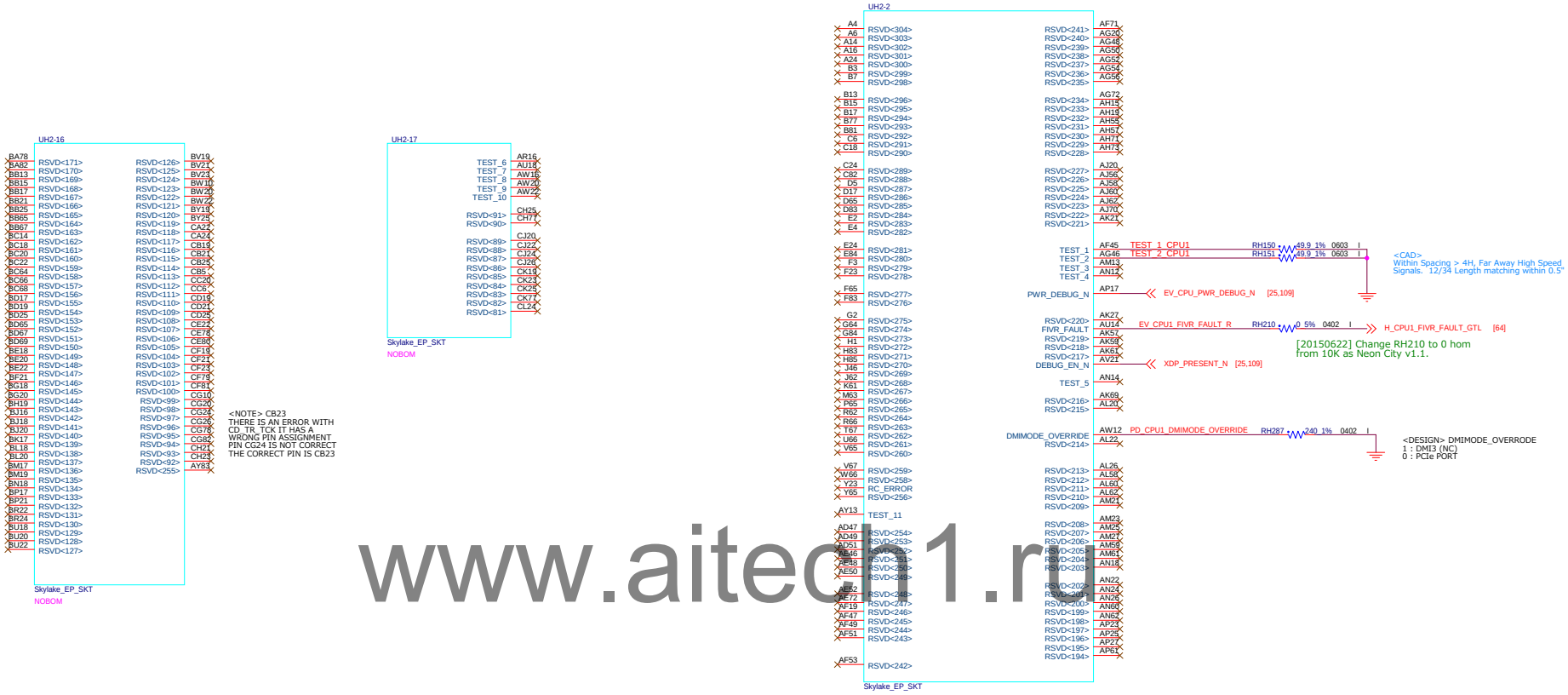
COMPRESSED IMAGE



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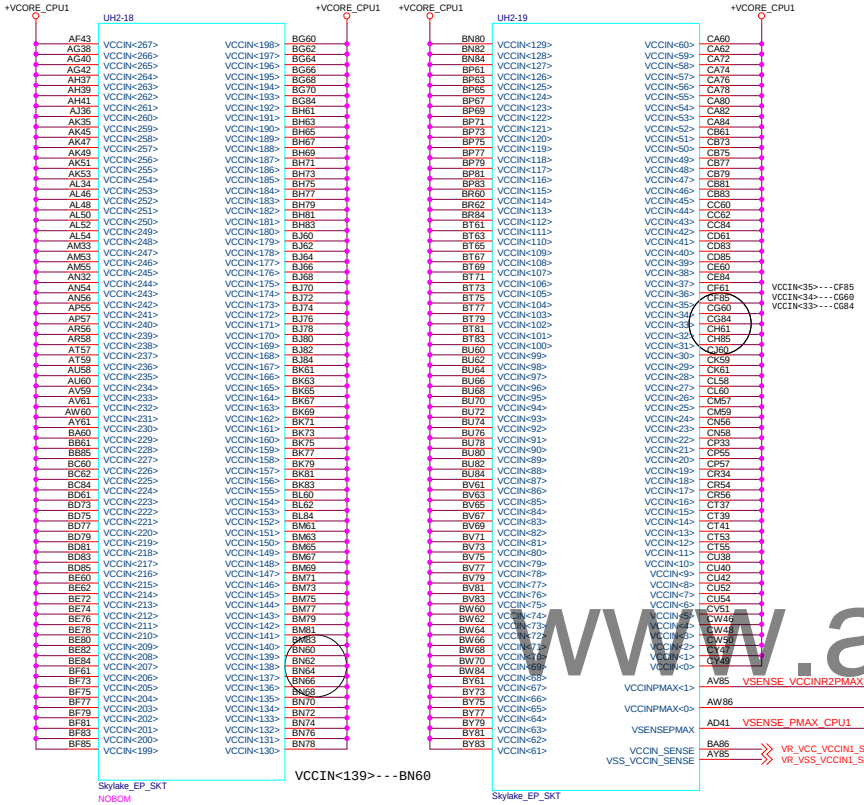
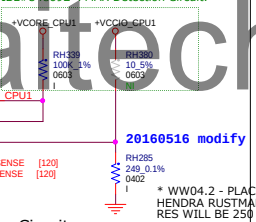
TITLE	CPU1 Test/Rsvd
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	47 of 150

COMPRESSED IMAGE



[20150612] Cange RH339 to 100K_1% from 100ohm and add RH380 10_5%(0603) PU to VccIO to reference IBL#548692_PMAX Detection Circuit.



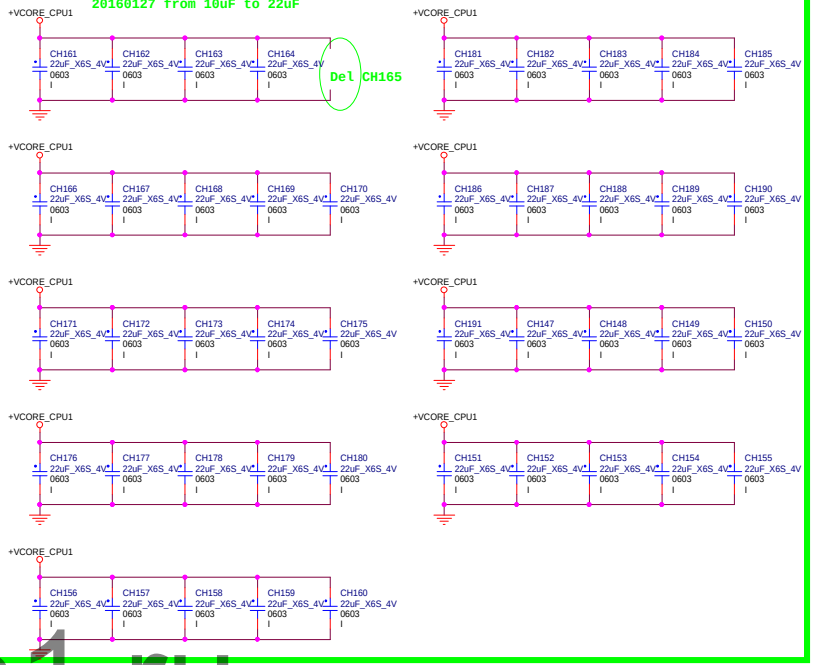
* WW04.2 - PLACE HOLDER
HENDRA RUSTMAN IS WORKING ON THIS RES WILL BE 250 0.1%

Pmax Detection Circuit

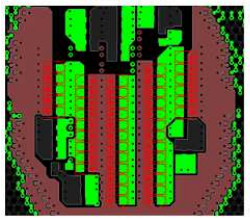
Enable	Disabled
RSense-Unstuffed (RH380)	RSense-Populate (RH380)

CPU1 VccIN VR13.0 Output Caps (Top Socket Cavity)

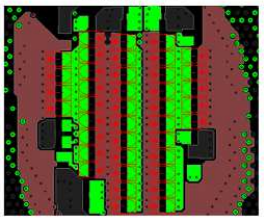
<CAD>TOP LAYER AT THE SOCKET CAVITY



Skt cavity caps
Top layer
45 x0603 10uF

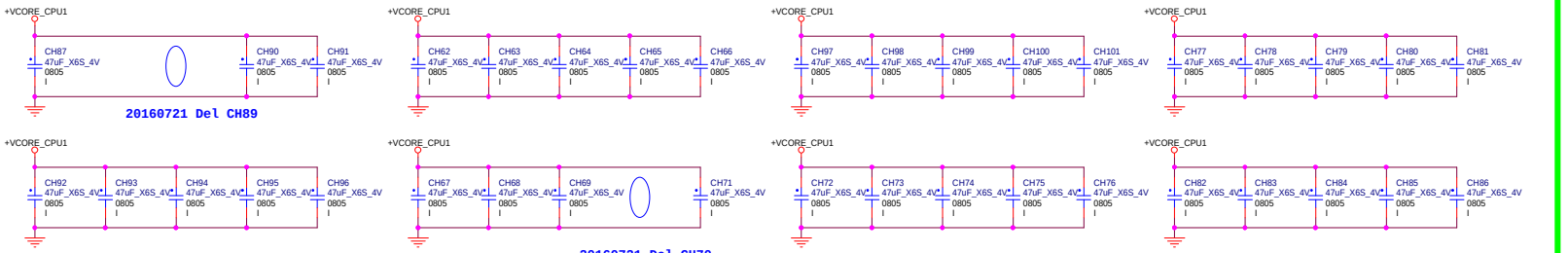


Skt cavity caps
Bot layer
40 x0805 22uF



CPU1 VccIN VR13.0 Output Caps (Bottom Socket Cavity) 20160127 from 22uF to 47 uF

<CAD> BOTTOM LAYER OF THE SOCKET CAVITY



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TITLE	CPU1 PWR-VCCIN
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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COMPRESSED IMAGE

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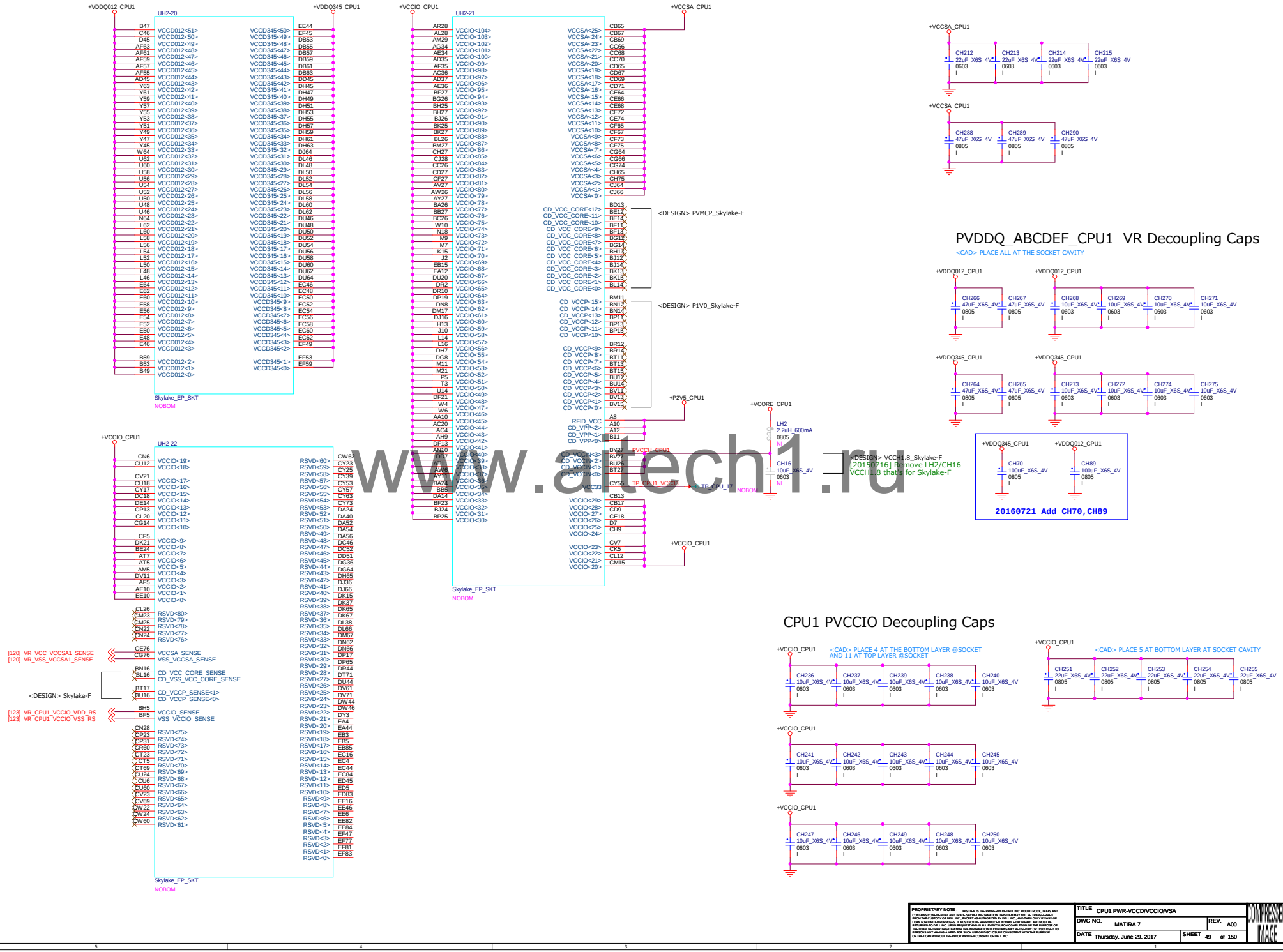

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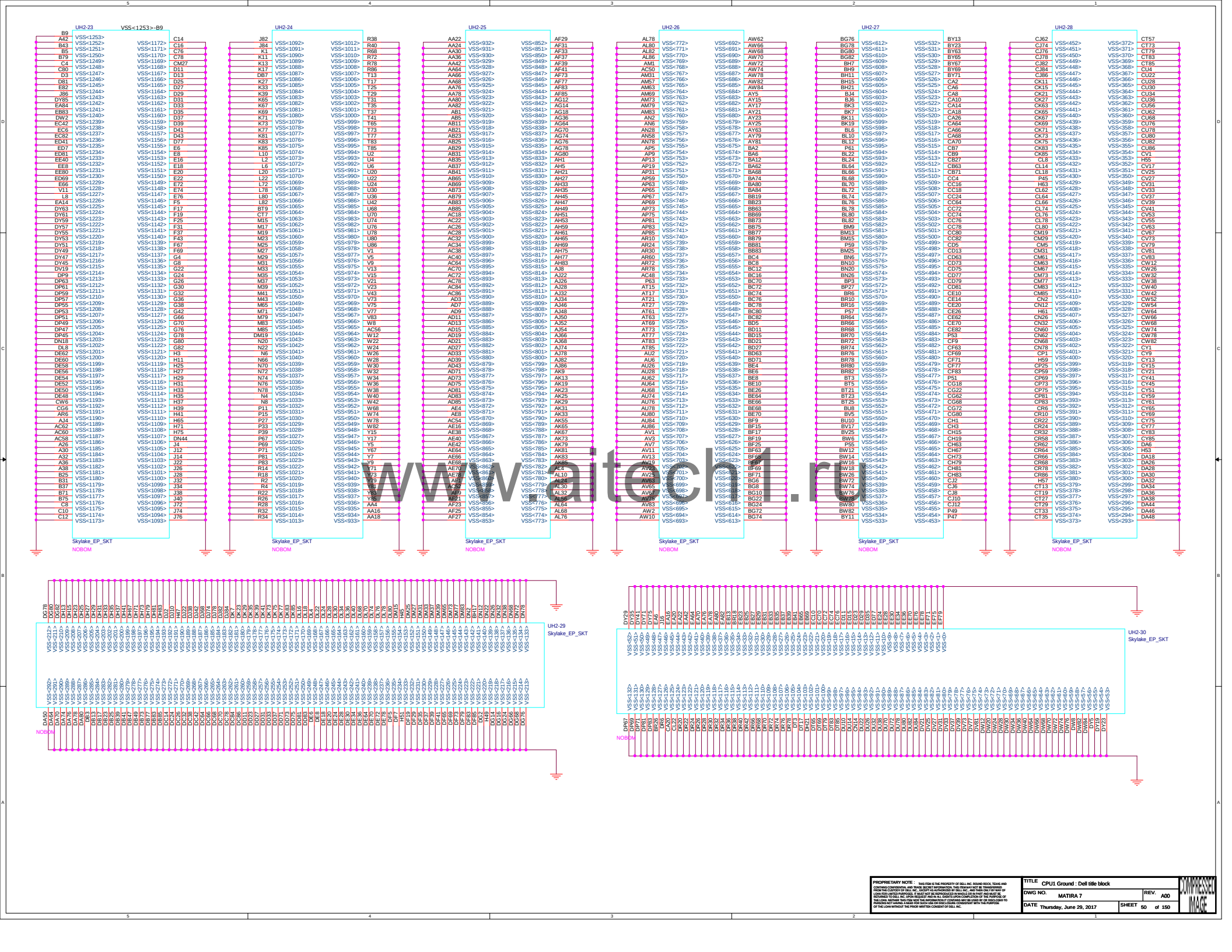
TITLE	CPU1 PWR-VCCD/VCCIO/VSA
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	49 of 150

UNCOMPRESSED IMAGE



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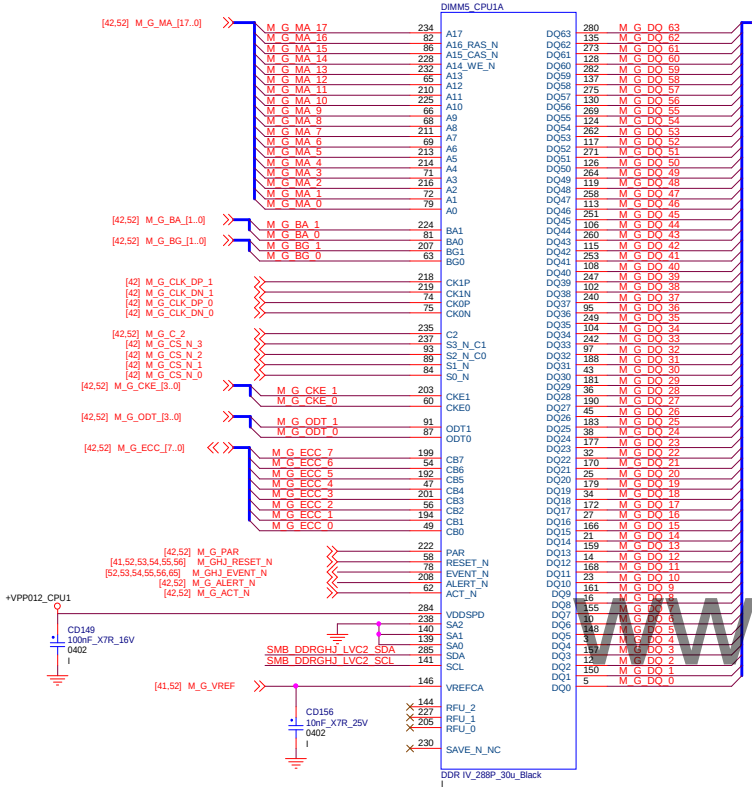
TITLE	CPU1 Ground : Dell title block
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	50 of 150

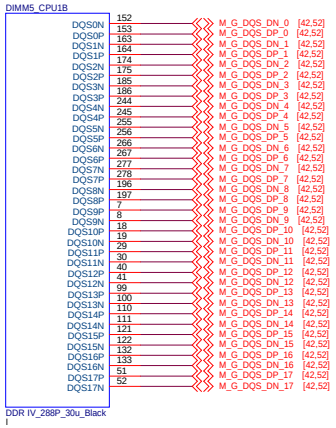
COMPRESSED IMAGE

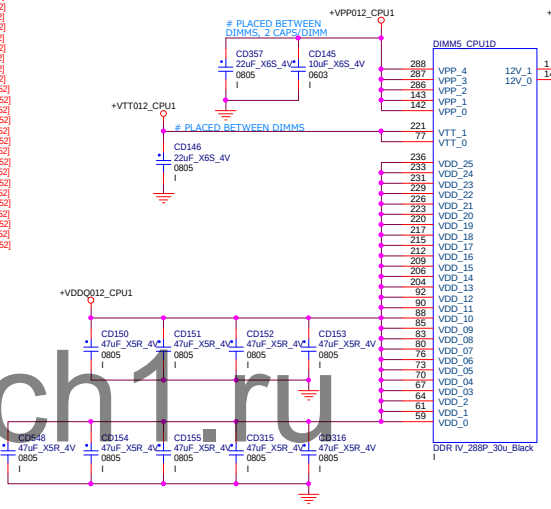
SA[2:0] = 000
SPD = 0xA0
TSOD = 0x30

DDR4 DIMM5 CPU1.CHG.D0



SPD I2C ID = A0

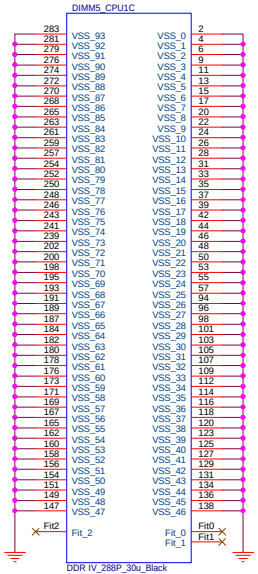


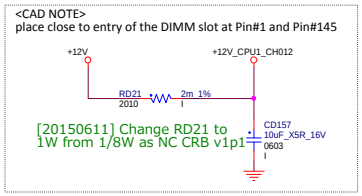


CPU0 PVCCIO Decoupling Caps

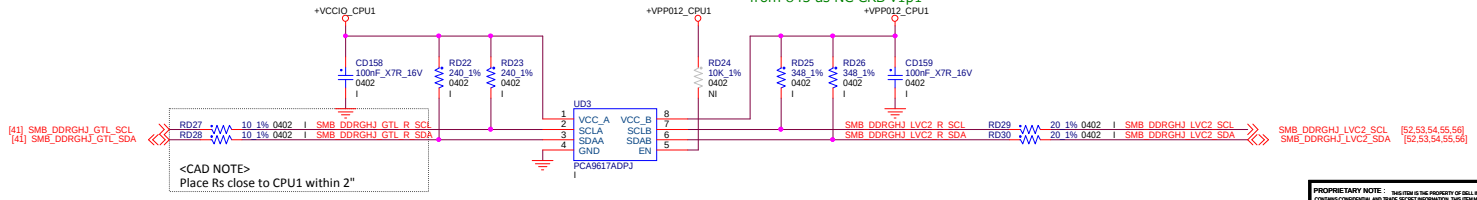
PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6





[20150623] Change RD25/26 to 348 from 845 as NC CRB v1p1



CHECK PDG

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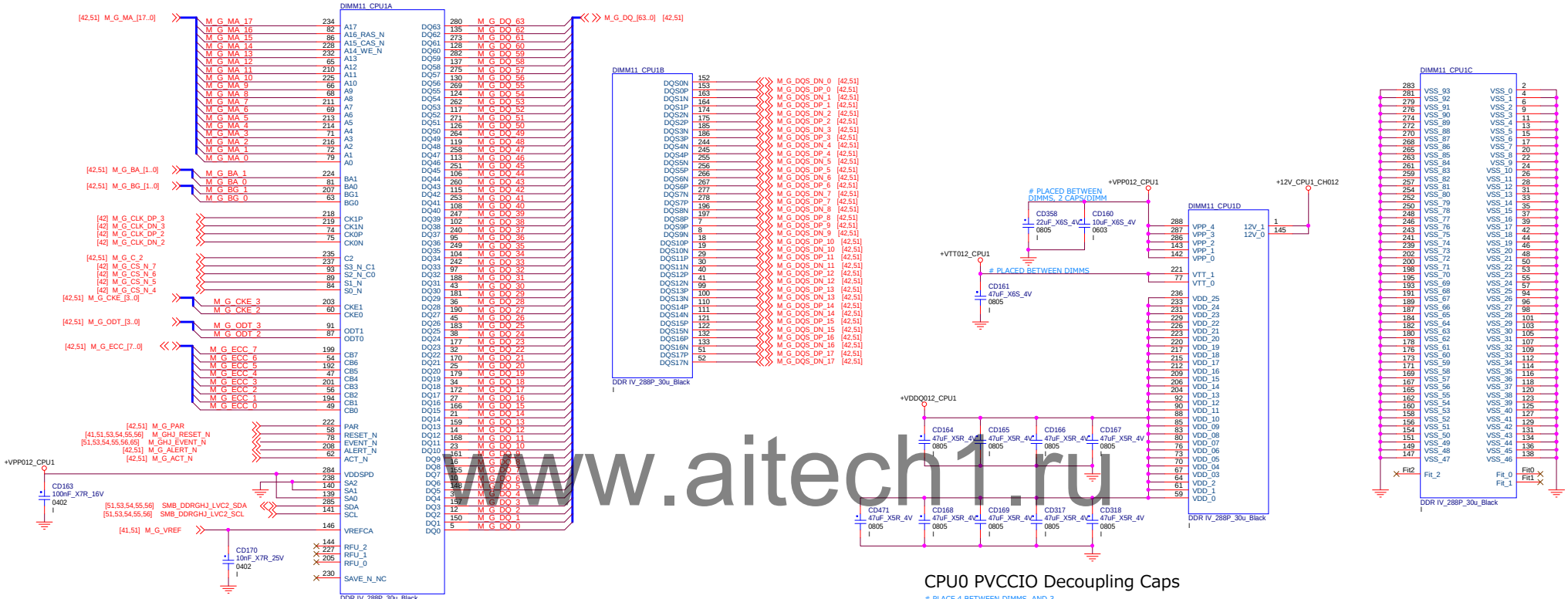
TITLE	DDR4 DIMM5 CPU1.CHG.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	51 of 150

COMPRESSED IMAGE

SA[2:0] = 001
SPD = 0xA2
TSOD = 0x32

DDR4 DIMM11 CPU1.CHG.D1



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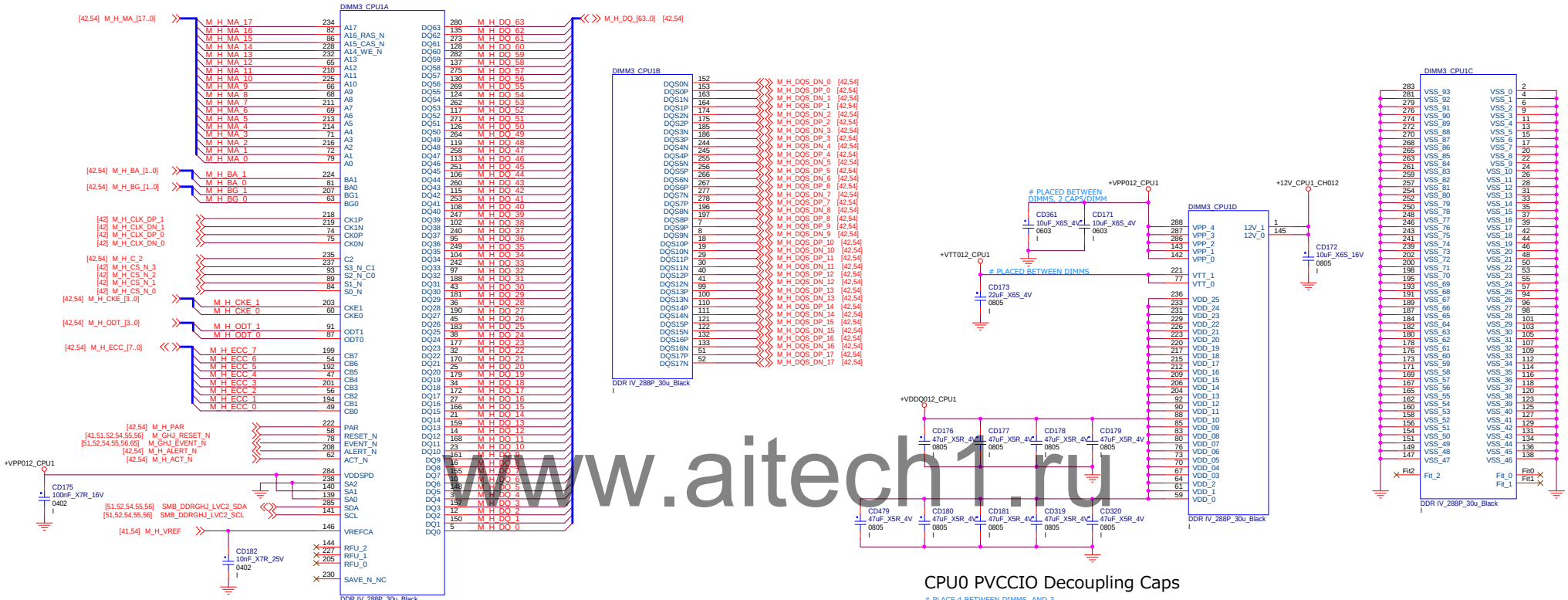
TITLE	DDR4 DIMM11 CPU1.CHG.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	52 of 150

COMPRESSED IMAGE

SA[2:0] = 010
SPD = 0xA4
TSOD = 0x34

DDR4 DIMM3 CPU1.CHH.D0



SPD I2C ID = A4

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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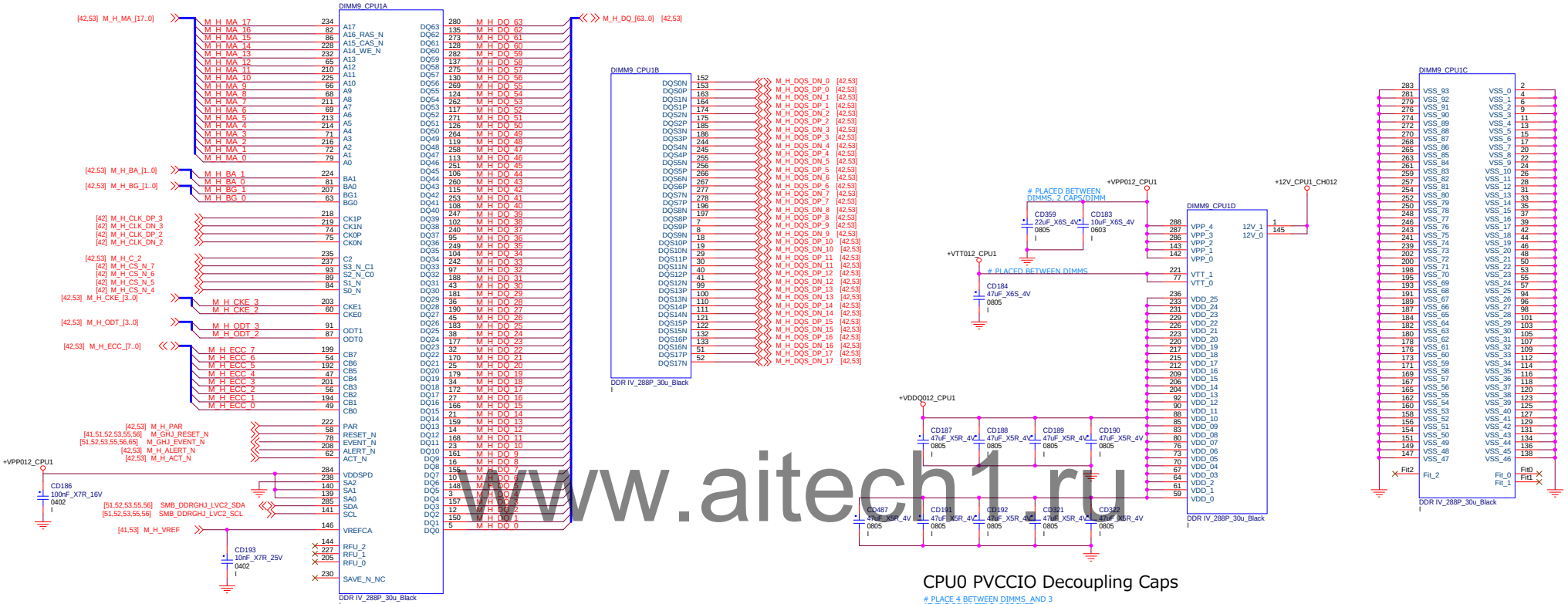
TITLE	DDR4 DIMM3 CPU1.CHH.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	53 of 150

COMPRESSED IMAGE

SA[2:0] = 011
SPD = 0xA6
TSOD = 0x36

DDR4 DIMM9 CPU1.CHH.D1



SPD I2C ID = A6

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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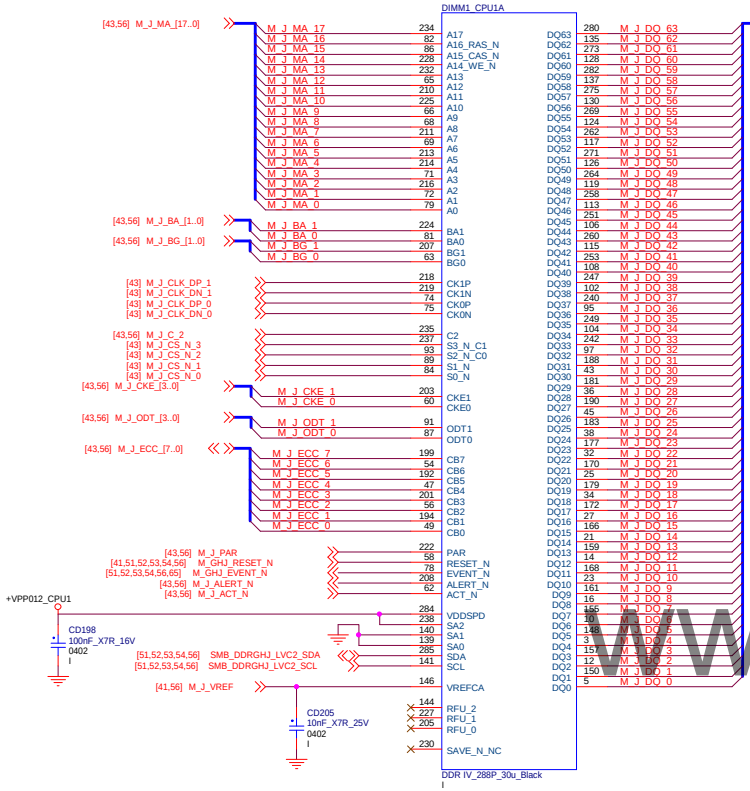
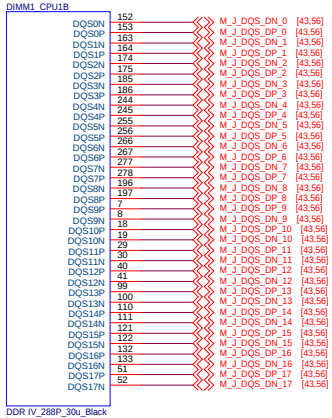
TITLE	DDR4 DIMM9 CPU1.CHH.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	54 of 150

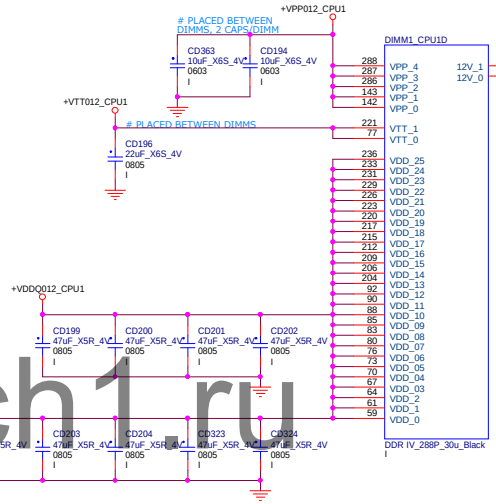
COMPRESSED IMAGE

SA[2:0] = 101
SPD = 0xA8
TSOD = 0x38

DDR4 DIMM1 CPU1.CHJ.D0



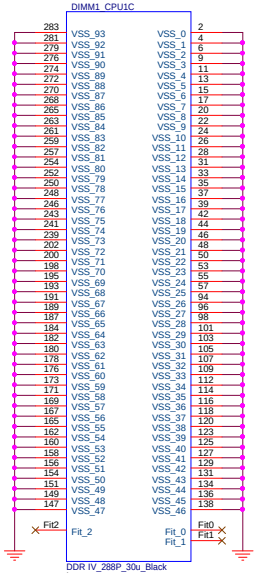




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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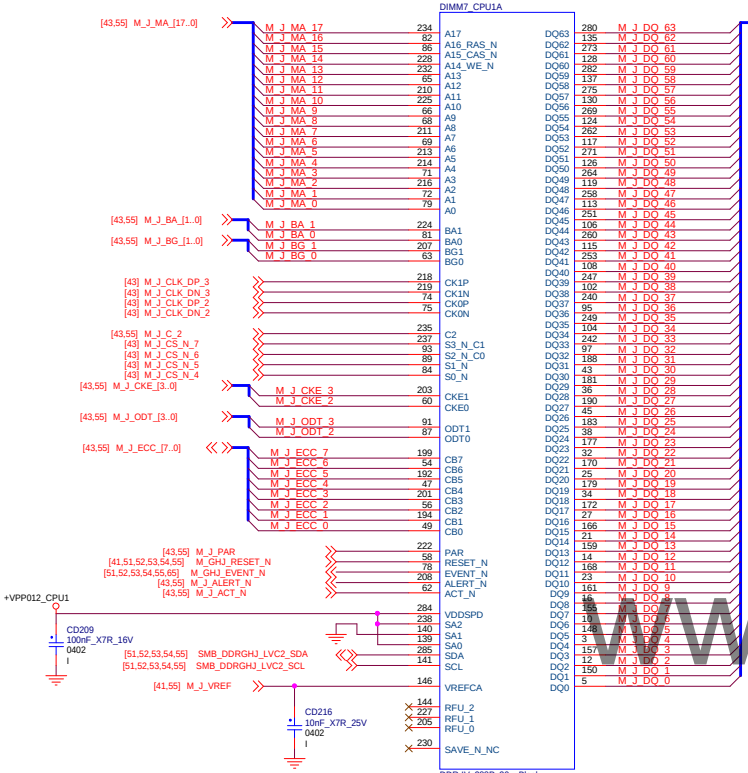
TITLE	DDR4 DIMM1 CPU1.CHJ.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	55 of 150

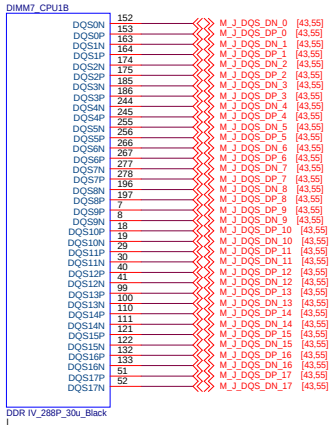
COMPRESSED IMAGE

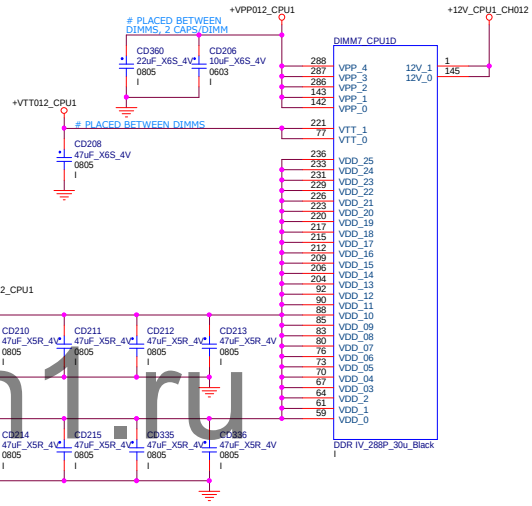
SA[2:0] = 101
SPD = 0xAA
TSOD = 0x3A

DDR4 DIMM7 CPU1.CHJ.D1



SPD I2C ID = AA

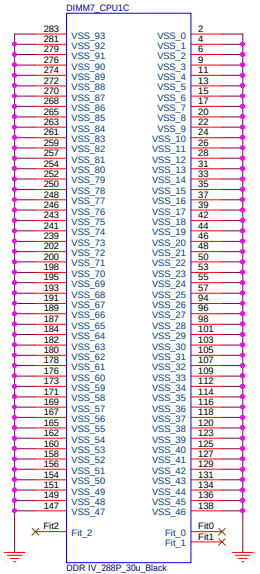




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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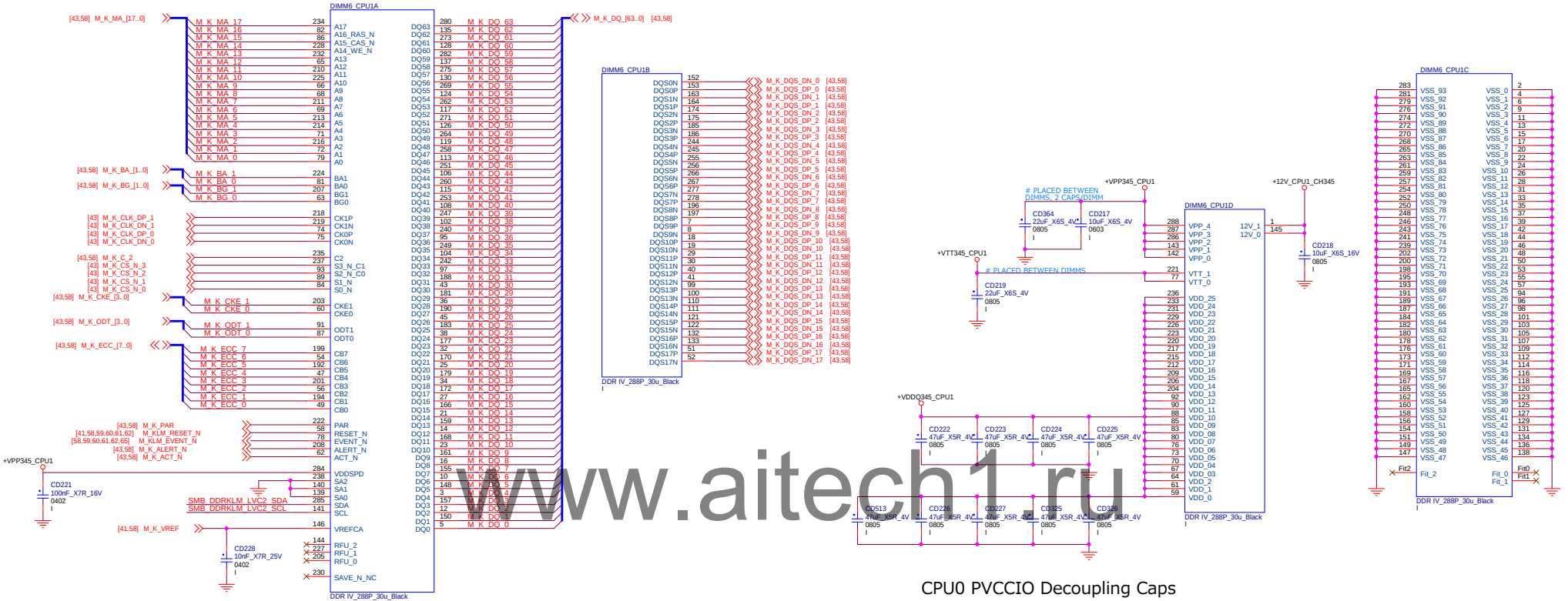
TITLE DDR4 DIMM7 CPU1.CHJ.D1
DWG NO. MATIRA 7
REV. A00
DATE Thursday, June 29, 2017
SHEET 56 of 150

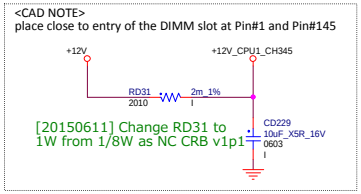
COMPRESSED IMAGE

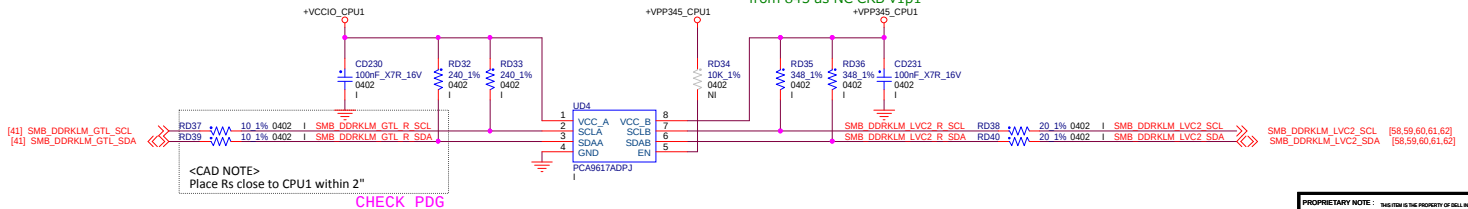
SA[2:0] = 000
SPD = 0xA0
TSOD = 0x30

DDR4 DIMM6 CPU1.CHK.D0



www.aitech1.ru





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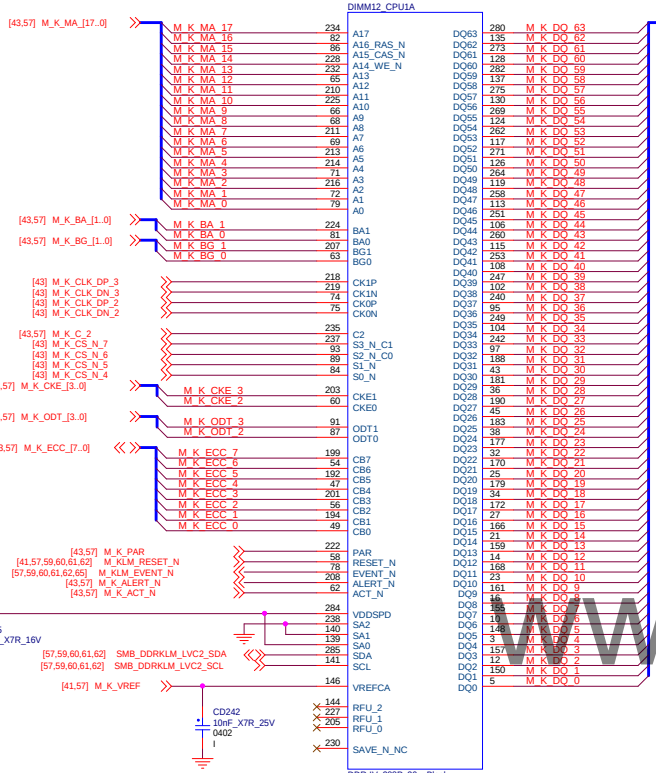
TITLE	DDR4 DIMM6 CPU1.CHK.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	57 of 150

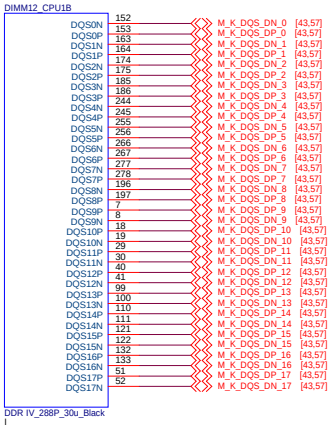
COMPRESSED IMAGE

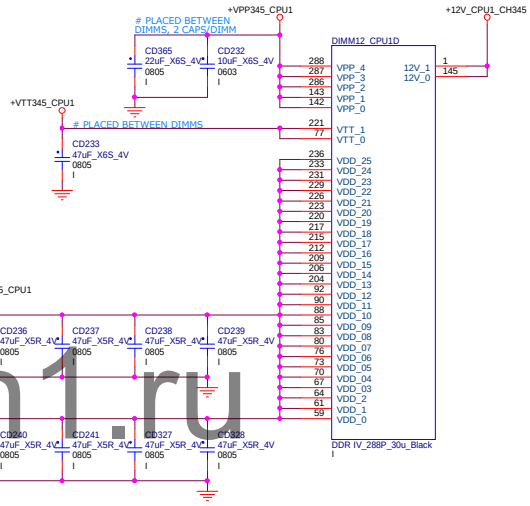
SA[2:0] = 001
SPD = 0xA2
TSOD = 0x32

DDR4 DIMM12 CPU1.CHK.D1



SPD I2C ID = A2

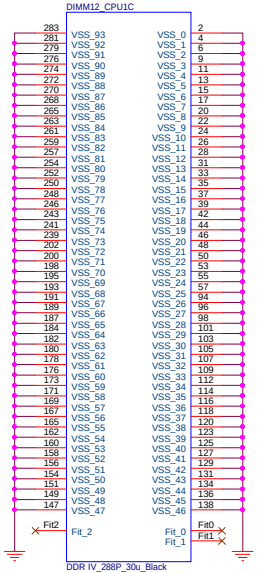




CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS_AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



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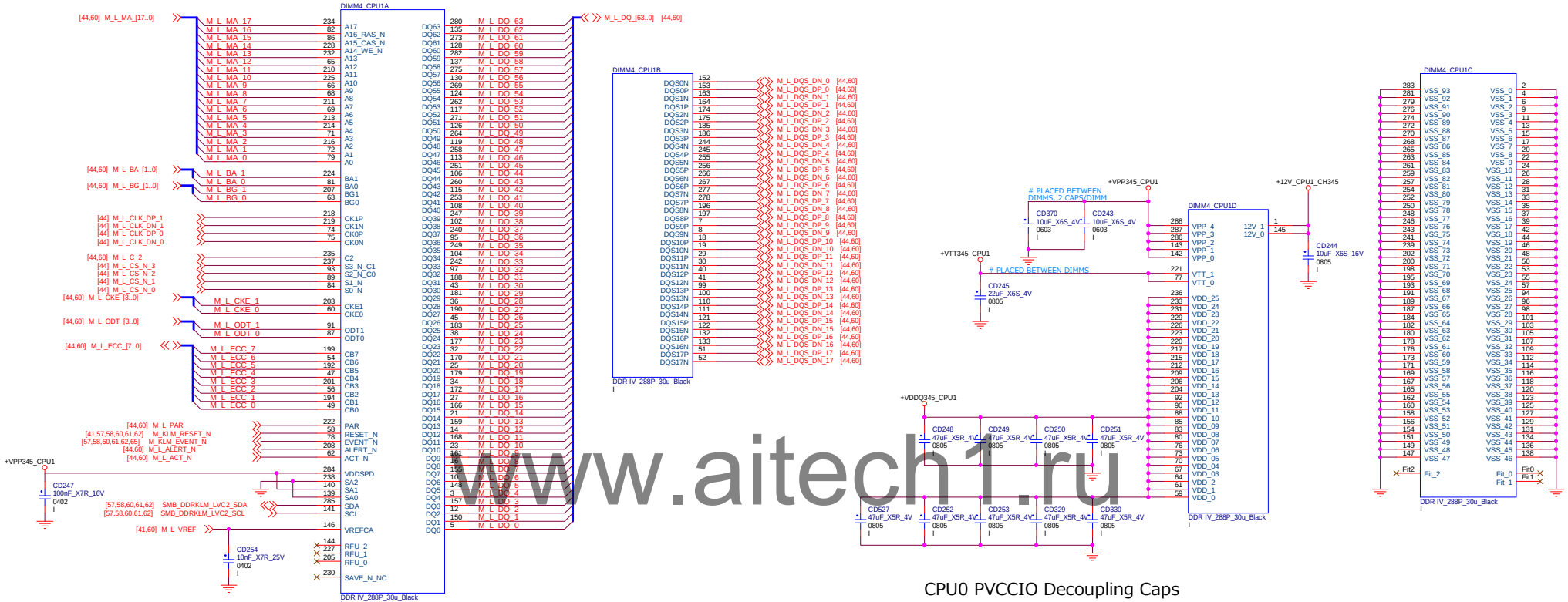
TITLE DDR4 DIMM12 CPU1.CHK.D1
DWG NO. MATIRA 7
REV. A00
DATE Thursday, June 29, 2017
SHEET 58 of 150

COMPRESSED IMAGE

SA[2:0] = 010
SPD = 0xA4
TSOD = 0x34

DDR4 DIMM4 CPU1.CHL.D0



SPD I2C ID = A4

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS_AND 3 AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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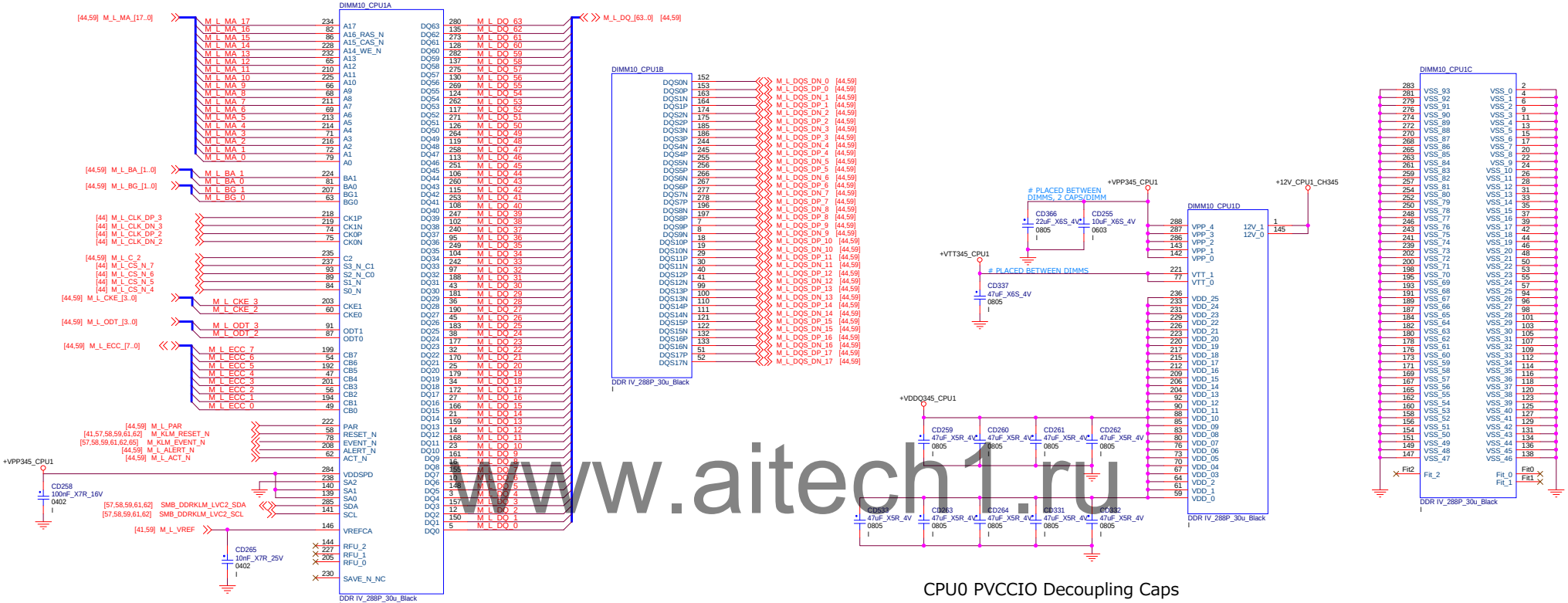
TITLE	DDR4 DIMM4 CPU1.CHL.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	59 of 150

COMPRESSED IMAGE

SA[2:0] = 011
SPD = 0xA6
TSOD = 0x36

DDR4 DIMM10 CPU1.CHL.D1



SPD I2C ID = A6

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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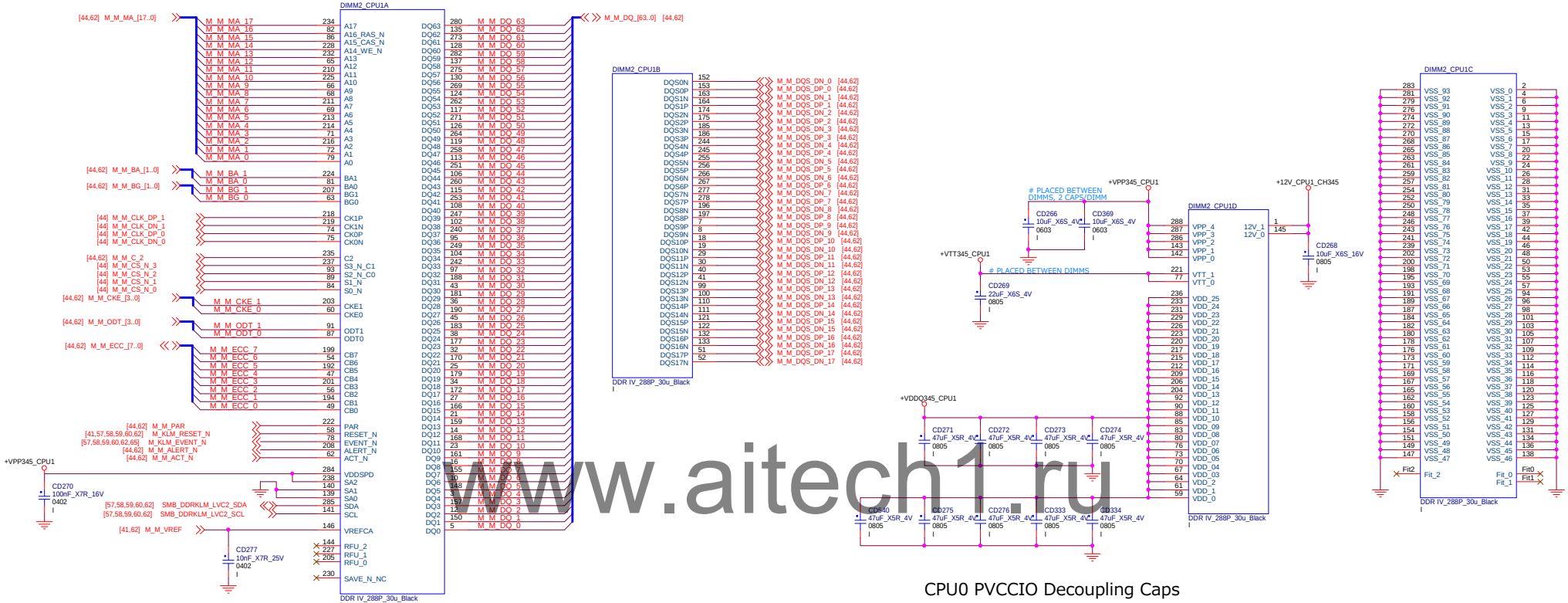
TITLE	DDR4 DIMM10 CPU1.CHL.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	60 of 150

COMPRESSED IMAGE

SA[2:0] = 100
SPD = 0xA8
TSOD = 0x38

DDR4 DIMM2 CPU1.CHM.D0



SPD I2C ID = A8

CPU0 PVCCIO Decoupling Caps

PLACE 4 BETWEEN DIMMS AND 3
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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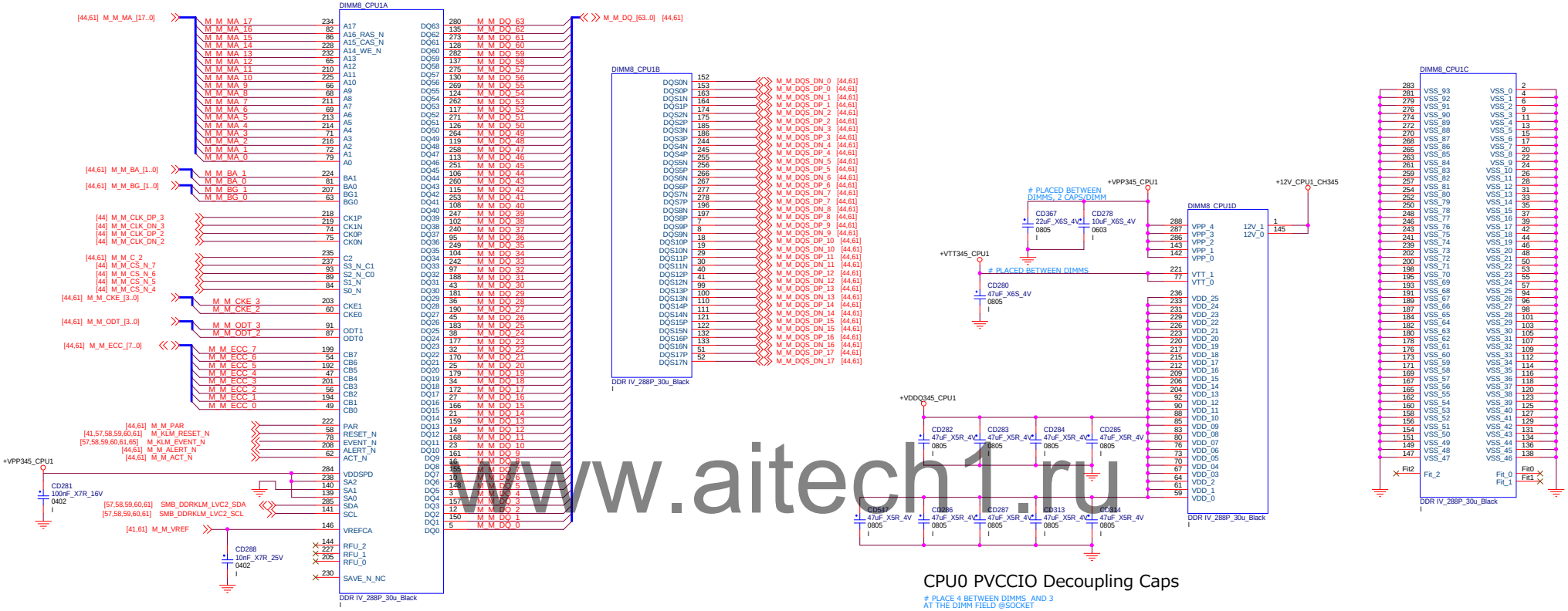
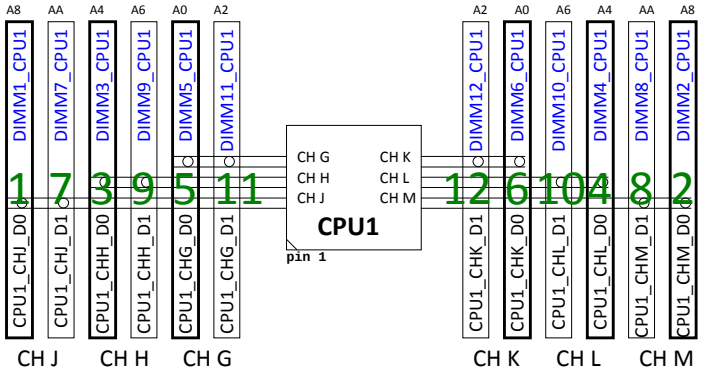
TITLE	DDR4 DIMM2 CPU1.CHM.D0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	61 of 150

COMPRESSED IMAGE

SA[2:0] = 101
SPD = 0xAA
TSOD = 0x3A

DDR4 DIMM8 CPU1.CHM.D1





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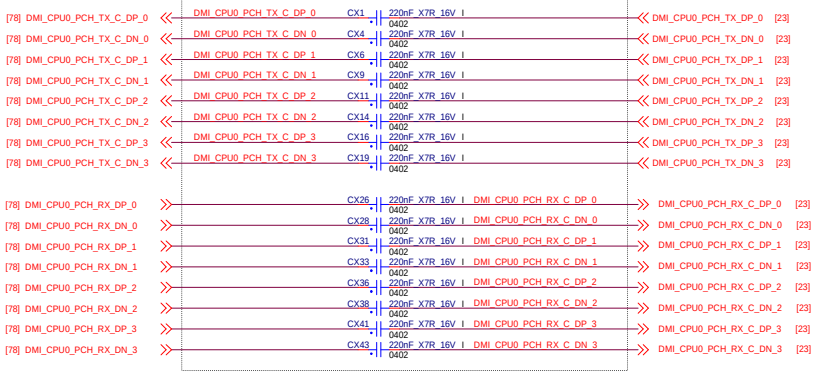
TITLE	DDR4 DIMM8 CPU1.CHM.D1
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	62 of 150

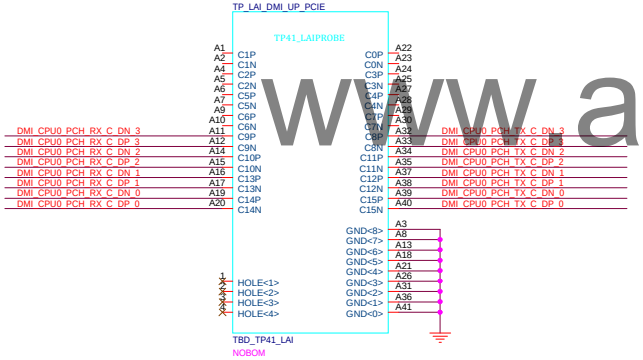
COMPRESSED IMAGE

DMI

Midbus Footprint



DMI/UPLINK LAI Connector Need check signal P/N



Follow CRB (BSC)

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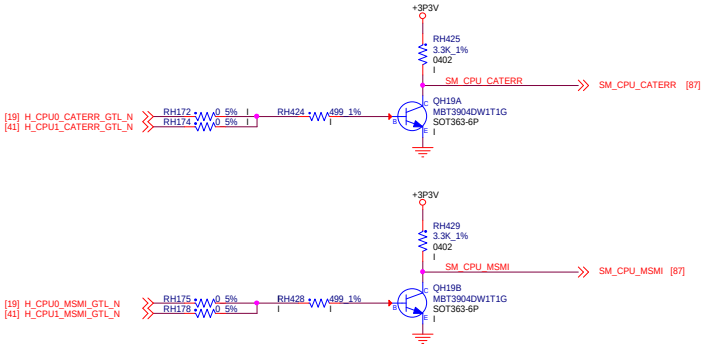
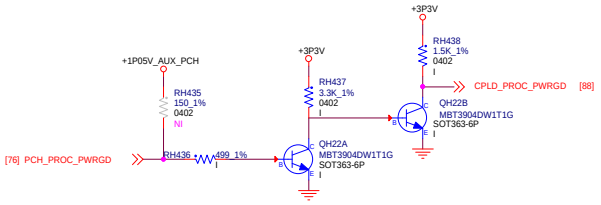
TITLE	DMI_LAI/UPLINK
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	63 of 150

COMPRESSED IMAGE

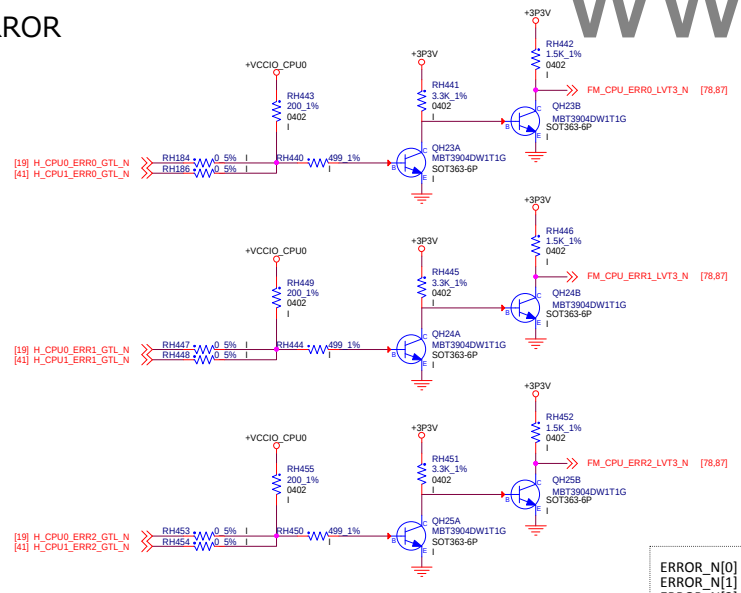
CRTERR / MSMI / EAR / CPU PG



20160315 del FM_CPU0_EAR_G_N,FM_CPU1_EAR_G_N,FM_CPU_EAR_LVT_N peripheral component

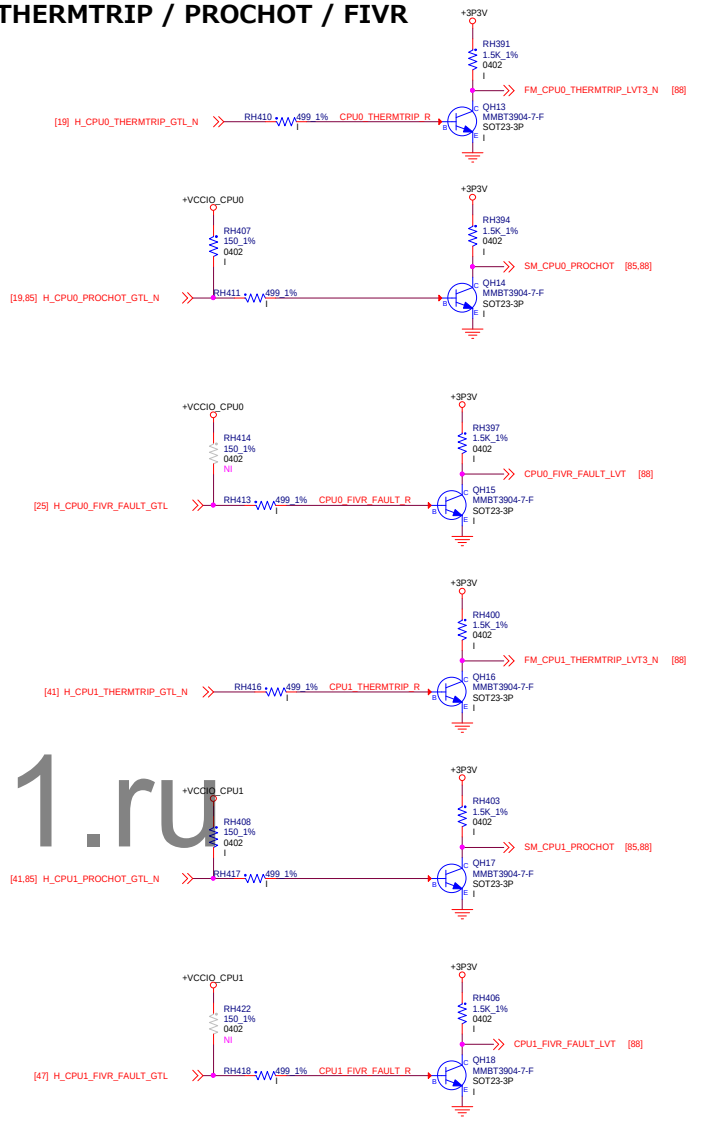


ERROR



ERROR_N[0] = EC/ PCH
ERROR_N[1] = EC/ PCH
ERROR_N[2] = EC/ PCH

THERMTRIP / PROCHOT / FIVR



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TITLE	CPU Common Logic - 1OF2	
DWG NO.	MATIRA 7	REV. A00
DATE	Thursday, June 29, 2017	SHEET 64 of 150

COMPRESSED IMAGE

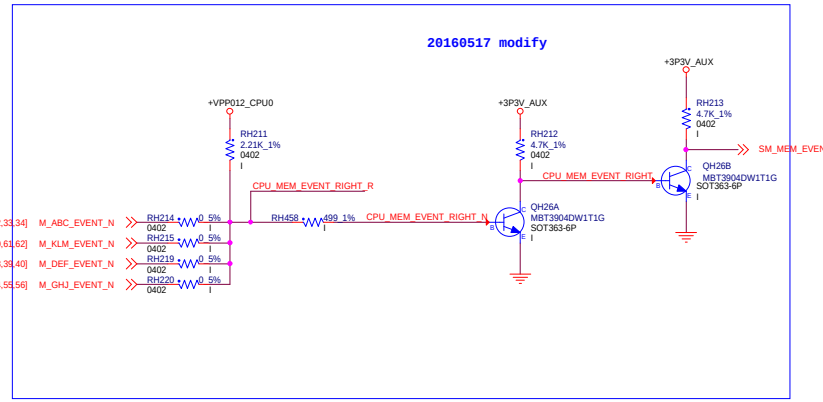
HOT

20160517 delete
EC do this function

NOTE :
Input : asserted by the platform and is used to detect external events such as VR_HOT# from the memory voltage regulators and cause the processor to throttle the memory channel.

Output : internally asserted and has two modes - level mode and duty cycle mode.

MEM EVENT



CPU PG / CPU RST

20160517 delete
CPLD connect to CPU directly

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MEM PG

20160517 delete
CPLD connect to CPU directly

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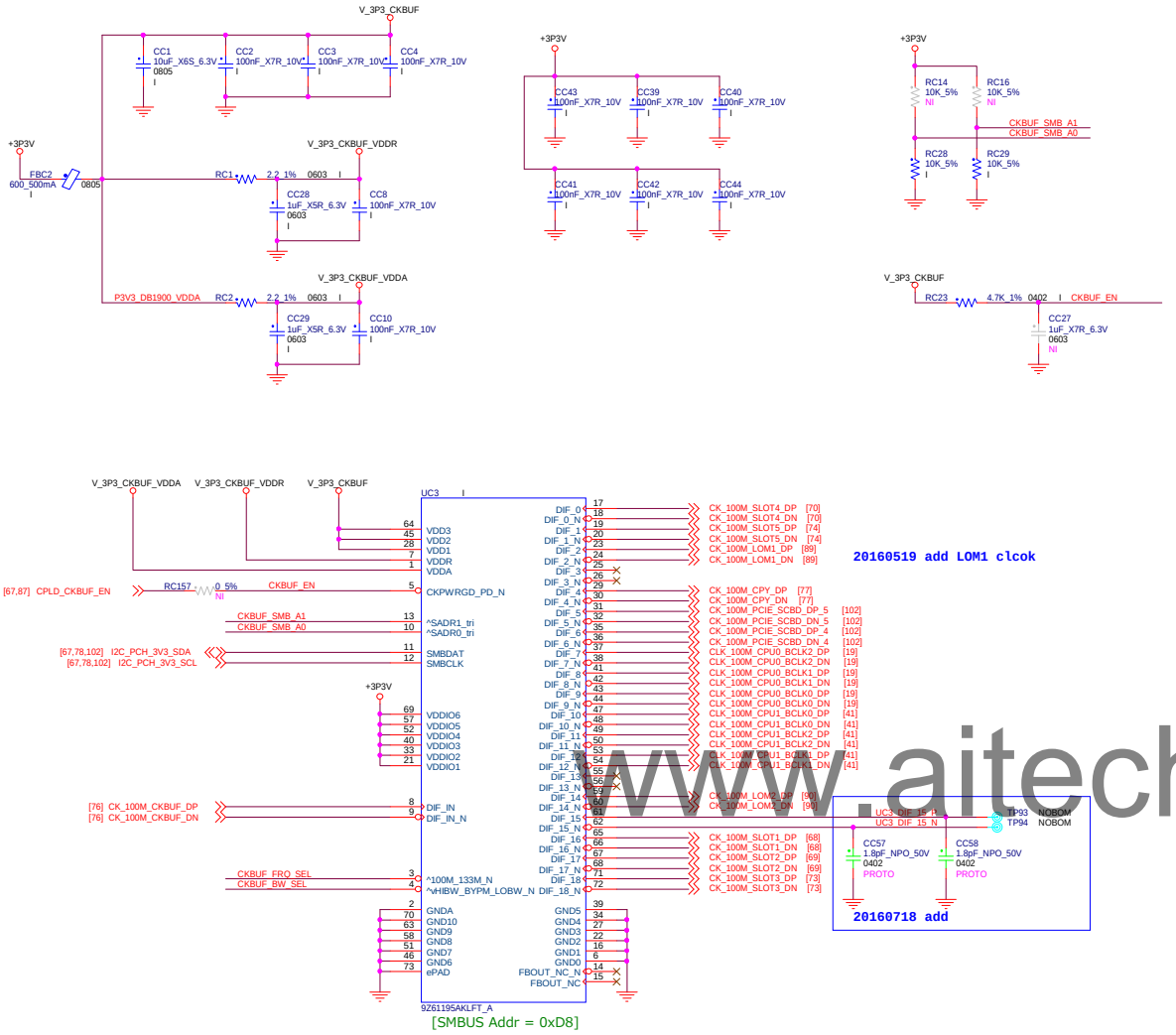
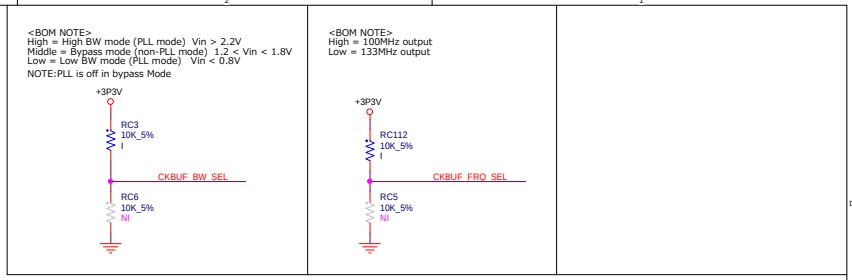
TITLE	CPU Common Logic - 2OF2		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	65 of 150

COMPRESSED IMAGE





Clock Port Assignment (PCH Hybride Mode)

Source from PCH

Clock Name	Frequency	Clock Sink Devices
DIFF_0_P/N	100MHz, SSC Diff	PCIE Expansion Slot4 (CPU0)
DIFF_1_P/N	100MHz, SSC Diff	PCIE Expansion Slot5 (PCH)
DIFF_2_P/N	100MHz, SSC Diff	LOM1
DIFF_3_P/N	100MHz, SSC Diff	NA
DIFF_4_P/N	100MHz, SSC Diff	PCH CLKIN CPY
DIFF_5_P/N	100MHz, SSC Diff	PCIE-to-SSD Conn5
DIFF_6_P/N	100MHz, SSC Diff	PCIE-to-SSD Conn4
DIFF_7_P/N	100MHz, SSC Diff	CPU0 CLK2
DIFF_8_P/N	100MHz, SSC Diff	CPU0 CLK1
DIFF_9_P/N	100MHz, SSC Diff	CPU0 CLK0
DIFF_10_P/N	100MHz, SSC Diff	CPU1 CLK0
DIFF_11_P/N	100MHz, SSC Diff	CPU1 CLK2
DIFF_12_P/N	100MHz, SSC Diff	CPU1 CLK1
DIFF_13_P/N	100MHz, SSC Diff	NA
DIFF_14_P/N	100MHz, SSC Diff	LOM2
DIFF_15_P/N	100MHz, SSC Diff	NA
DIFF_16_P/N	100MHz, SSC Diff	PCIE Expansion Slot1 (CPU0)
DIFF_17_P/N	100MHz, SSC Diff	PCIE Expansion Slot2 (CPU0)
DIFF_18_P/N	100MHz, SSC Diff	PCIE Expansion Slot3 (PCH)

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LPC CLOCK BUFFER

20160426 del UF3

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TITLE	Clock Buffer 1/2
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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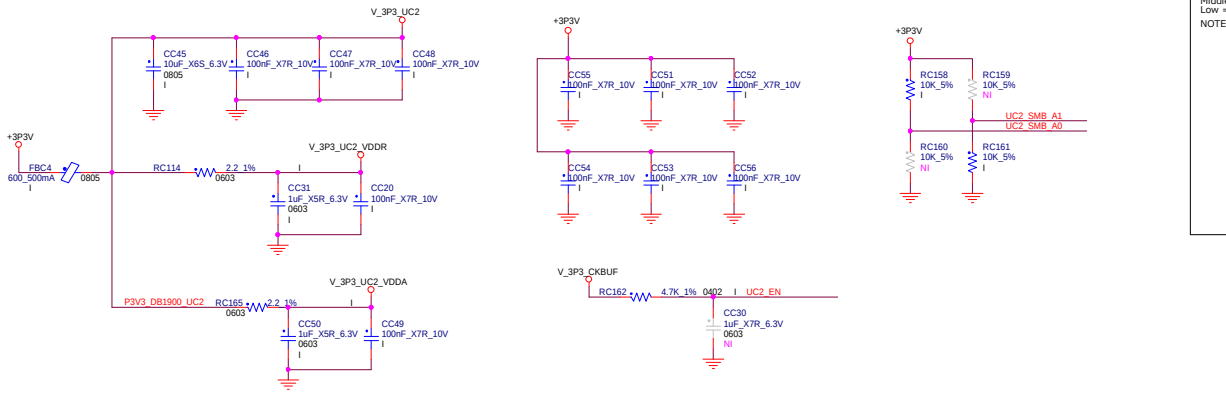
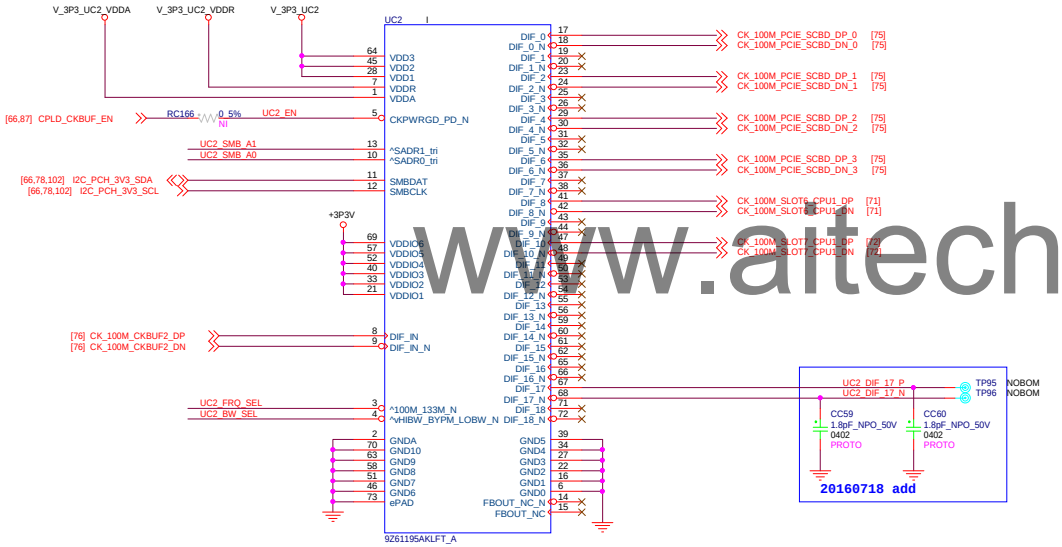
COMPRESSED IMAGE





[SMBUS Addr = 0xDE]

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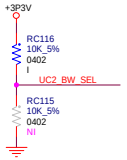
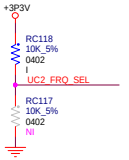
<BOM NOTE>
High = High BW mode (PLL mode) Vin > 2.2V
Middle = Bypass mode (non-PLL mode) 1.2 < Vin < 1.8V
Low = Low BW mode (PLL mode) Vin < 0.8V
NOTE:PLL is off in bypass Mode



<BOM NOTE>
High = 100MHz output
Low = 133MHz output



Clock Port Assignment (PCH Hybride Mode)

Source from PCH

Clock Name	Frequency	Clock Sink Devices
DIFF_0_P/N	100MHz, SSC Diff	CK_100M_PCIE_SCBD_0 (CPU0)
DIFF_1_P/N	100MHz, SSC Diff	CK_100M_PCIE_SCBD_1 (CPU0)
DIFF_2_P/N	100MHz, SSC Diff	CK_100M_PCIE_SCBD_2 (CPU1)
DIFF_3_P/N	100MHz, SSC Diff	CK_100M_PCIE_SCBD_3 (CPU1)
DIFF_4_P/N	100MHz, SSC Diff	PCIE Expansion Slot6 (CPU1)
DIFF_5_P/N	100MHz, SSC Diff	PCIE Expansion Slot7 (CPU1)
DIFF_6_P/N	100MHz, SSC Diff	NA
DIFF_7_P/N	100MHz, SSC Diff	NA
DIFF_8_P/N	100MHz, SSC Diff	NA
DIFF_9_P/N	100MHz, SSC Diff	NA
DIFF_10_P/N	100MHz, SSC Diff	NA
DIFF_11_P/N	100MHz, SSC Diff	NA
DIFF_12_P/N	100MHz, SSC Diff	NA
DIFF_13_P/N	100MHz, SSC Diff	NA
DIFF_14_P/N	100MHz, SSC Diff	NA
DIFF_15_P/N	100MHz, SSC Diff	NA
DIFF_16_P/N	100MHz, SSC Diff	NA
DIFF_17_P/N	100MHz, SSC Diff	NA
DIFF_18_P/N	100MHz, SSC Diff	NA

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TITLE	Clock Buffer 2/2
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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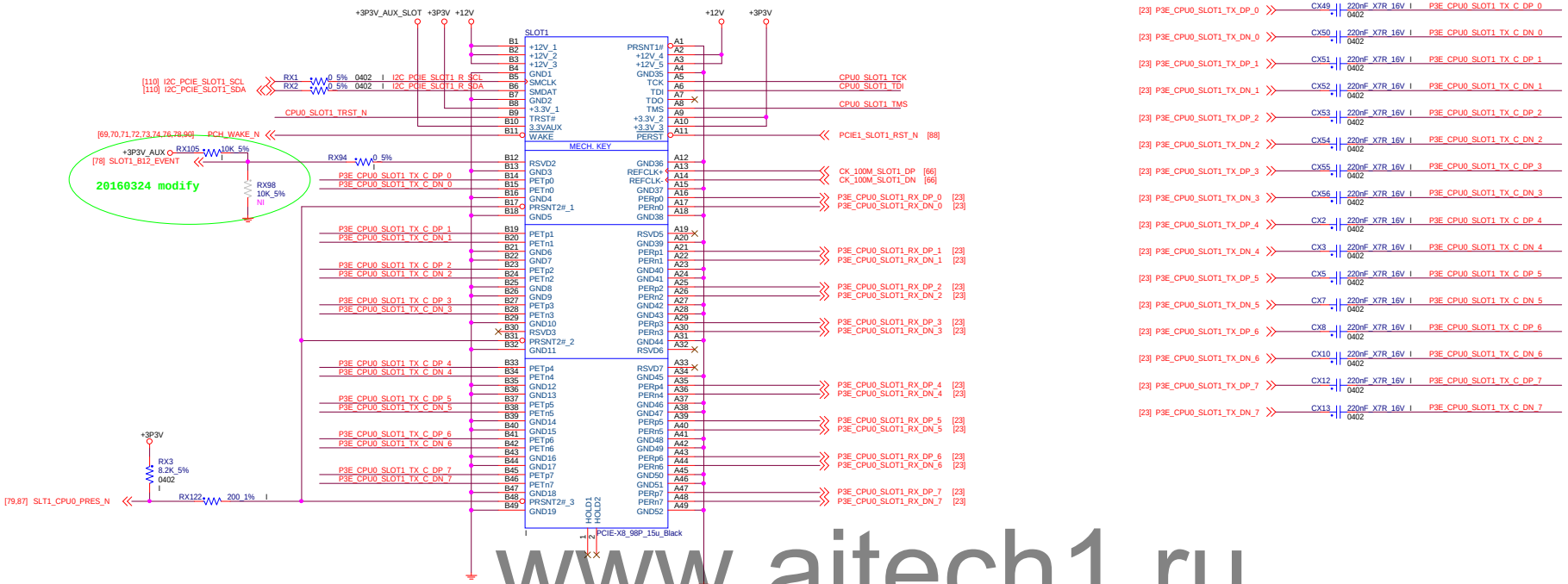
COMPRESSED IMAGE

PCIE x8 SLOT1 (CPU0 WIRED 8X GEN3)



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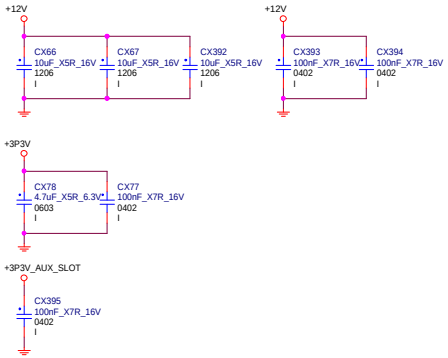

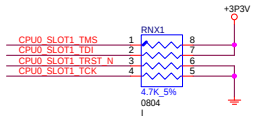

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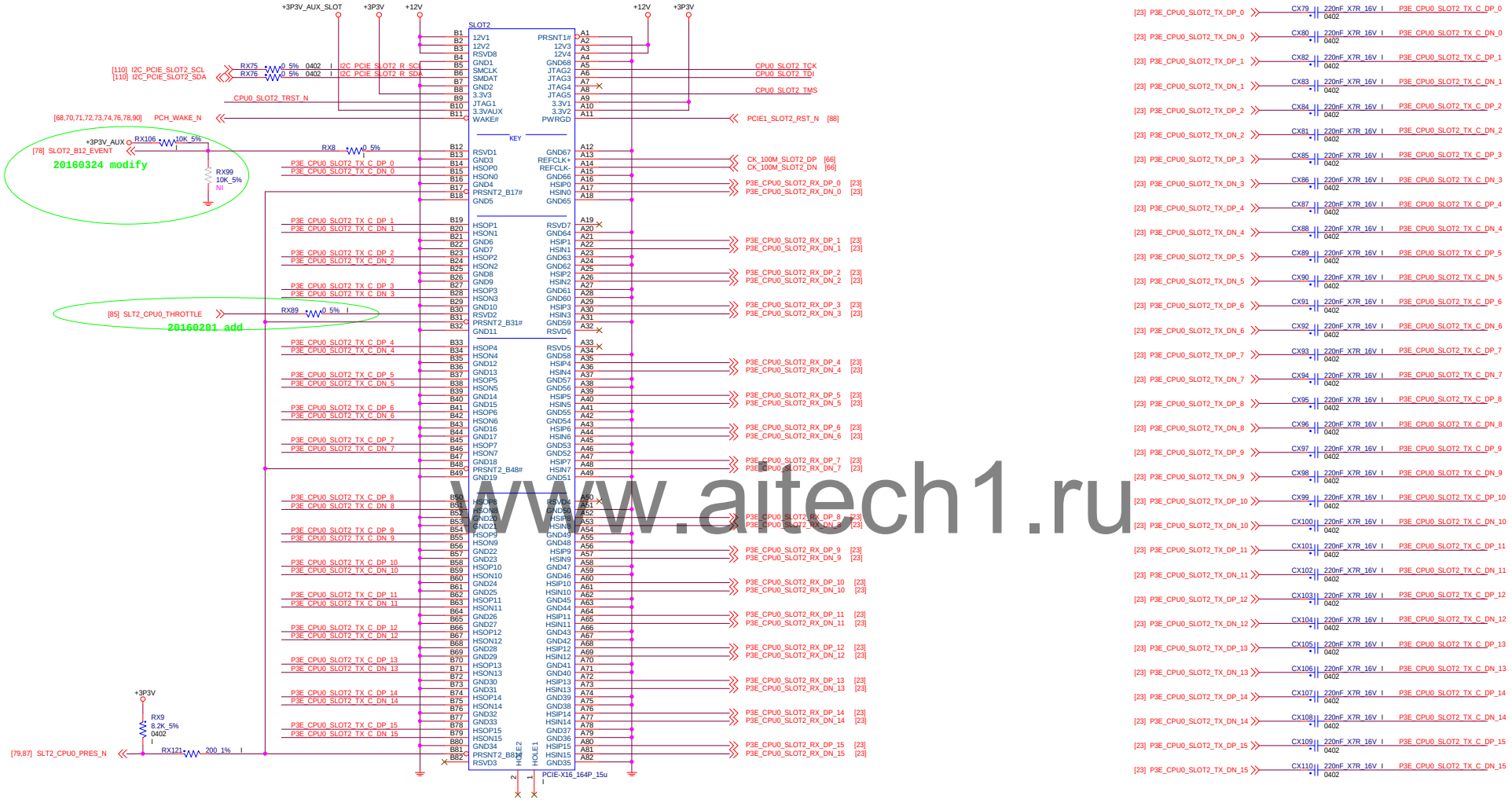
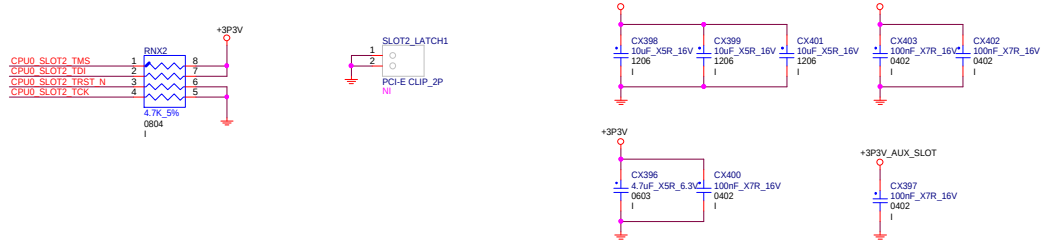
	DWG NO.: MATIRA 7	REV.: A00	
	DATE: Thursday, June 29, 2017	SHEET: 68 of 150	

COMPRESSED IMAGE

PCIE x16 SLOT2 (CPU0 WIRED 16X GEN3)





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TITLE	PCIE G3 X16-Slot2_CPU0
DWG NO.	MATIRA 7
REV.	A00
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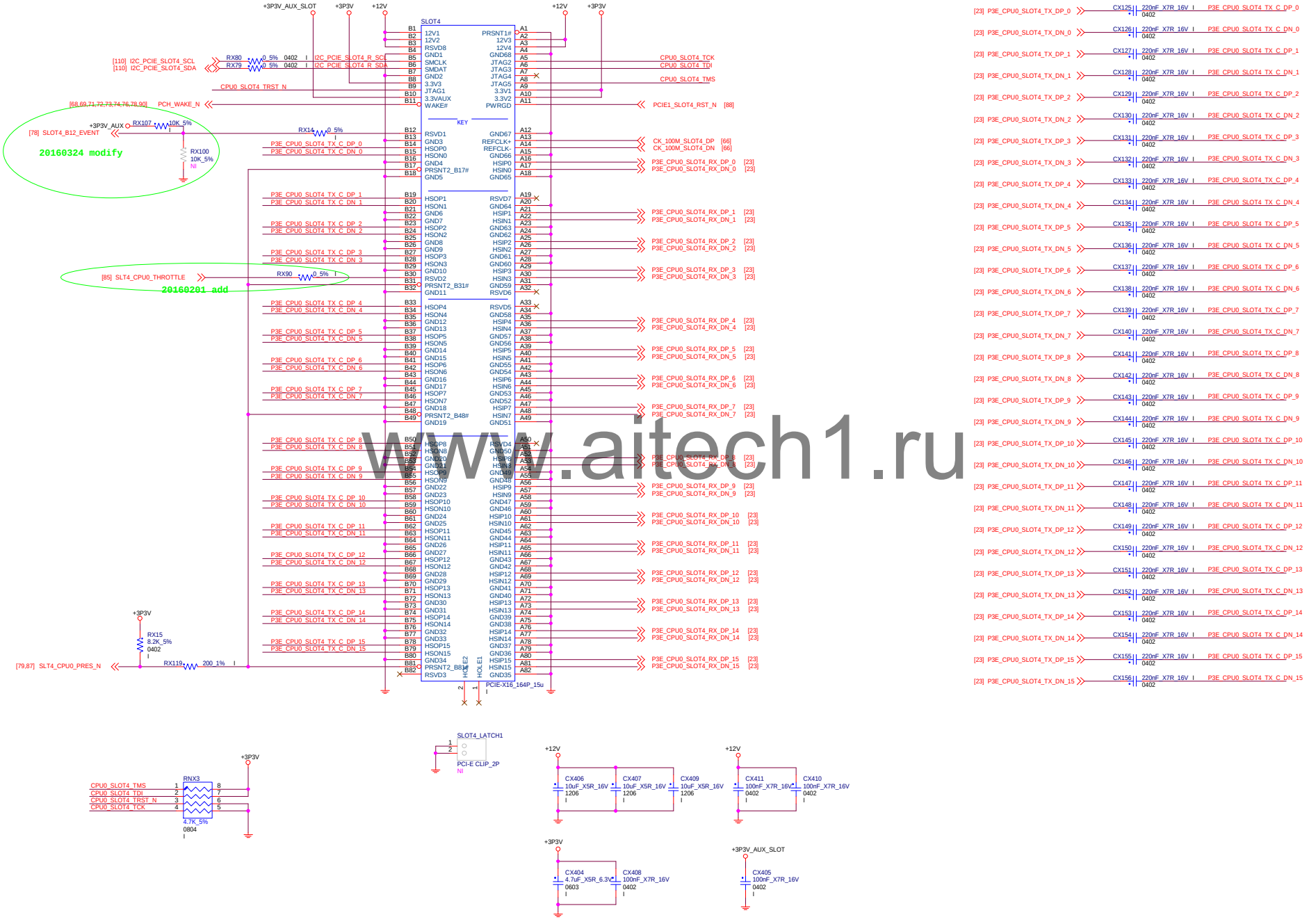
COMPRESSED IMAGE

PCIE x16 SLOT4 (CPU0 WIRED 16X GEN3)



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TITLE	PCIE G3 X16-Slot4_CPU0
DWG NO.	MATIRA 7
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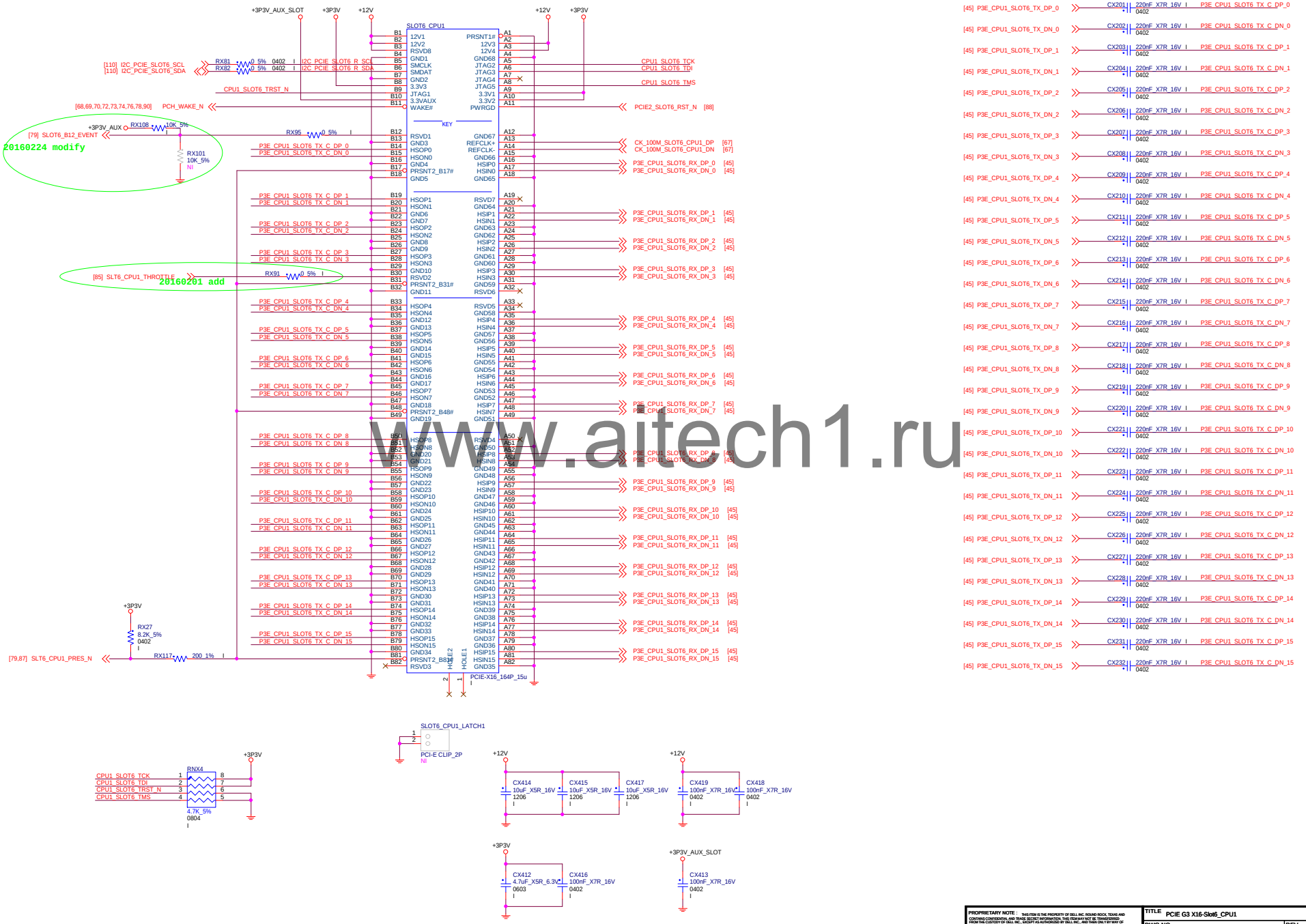
COMPRESSED IMAGE

PCIE x16 SLOT6 (CPU1 WIRED 16X GEN3)



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TITLE	PCIE G3 X16-Slot6_CPU1
DWG NO.	MATIRA 7
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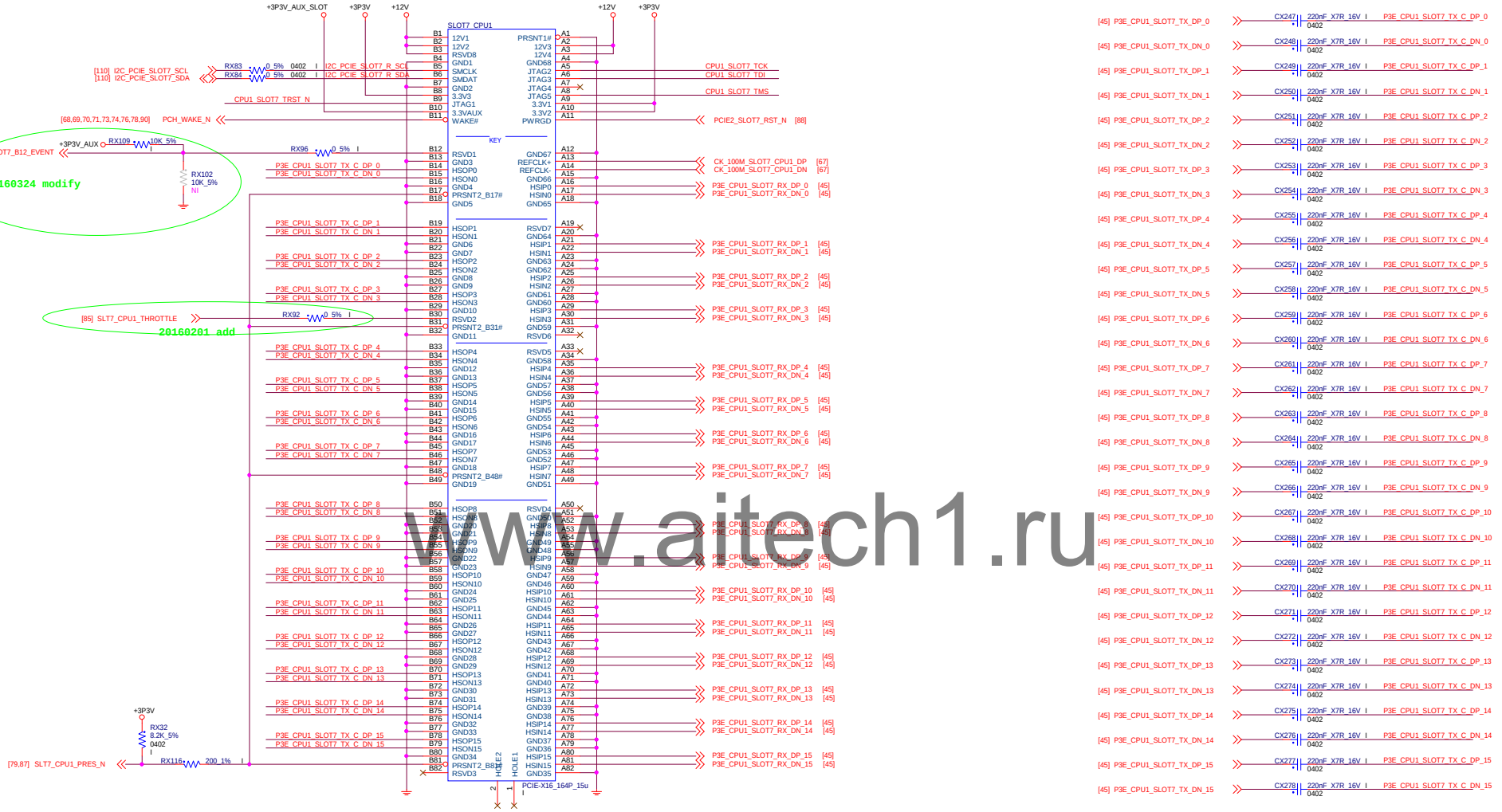
COMPRESSED IMAGE

PCIE x16 SLOT7 (CPU2 WIRED 16X GEN3)



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[45] P3E_CPU1_SLOT7_TX_DP_0	CX247	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_0
[45] P3E_CPU1_SLOT7_TX_DN_0	CX248	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_0
[45] P3E_CPU1_SLOT7_TX_DP_1	CX249	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_1
[45] P3E_CPU1_SLOT7_TX_DN_1	CX250	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_1
[45] P3E_CPU1_SLOT7_TX_DP_2	CX251	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_2
[45] P3E_CPU1_SLOT7_TX_DN_2	CX252	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_2
[45] P3E_CPU1_SLOT7_TX_DP_3	CX253	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_3
[45] P3E_CPU1_SLOT7_TX_DN_3	CX254	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_3
[45] P3E_CPU1_SLOT7_TX_DP_4	CX255	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_4
[45] P3E_CPU1_SLOT7_TX_DN_4	CX256	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_4
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[45] P3E_CPU1_SLOT7_TX_DN_5	CX258	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_5
[45] P3E_CPU1_SLOT7_TX_DP_6	CX259	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_6
[45] P3E_CPU1_SLOT7_TX_DN_6	CX260	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_6
[45] P3E_CPU1_SLOT7_TX_DP_7	CX261	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_7
[45] P3E_CPU1_SLOT7_TX_DN_7	CX262	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_7
[45] P3E_CPU1_SLOT7_TX_DP_8	CX263	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_8
[45] P3E_CPU1_SLOT7_TX_DN_8	CX264	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_8
[45] P3E_CPU1_SLOT7_TX_DP_9	CX265	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_9
[45] P3E_CPU1_SLOT7_TX_DN_9	CX266	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_9
[45] P3E_CPU1_SLOT7_TX_DP_10	CX267	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_10
[45] P3E_CPU1_SLOT7_TX_DN_10	CX268	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_10
[45] P3E_CPU1_SLOT7_TX_DP_11	CX269	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_11
[45] P3E_CPU1_SLOT7_TX_DN_11	CX270	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_11
[45] P3E_CPU1_SLOT7_TX_DP_12	CX271	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_12
[45] P3E_CPU1_SLOT7_TX_DN_12	CX272	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_12
[45] P3E_CPU1_SLOT7_TX_DP_13	CX273	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_13
[45] P3E_CPU1_SLOT7_TX_DN_13	CX274	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_13
[45] P3E_CPU1_SLOT7_TX_DP_14	CX275	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_14
[45] P3E_CPU1_SLOT7_TX_DN_14	CX276	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_14
[45] P3E_CPU1_SLOT7_TX_DP_15	CX277	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DP_15
[45] P3E_CPU1_SLOT7_TX_DN_15	CX278	220nF_X7R_16V 0402	P3E_CPU1_SLOT7_TX_C_DN_15

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TITLE	PCIE G3 X16-Slot7_CPU1
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REV.	A00
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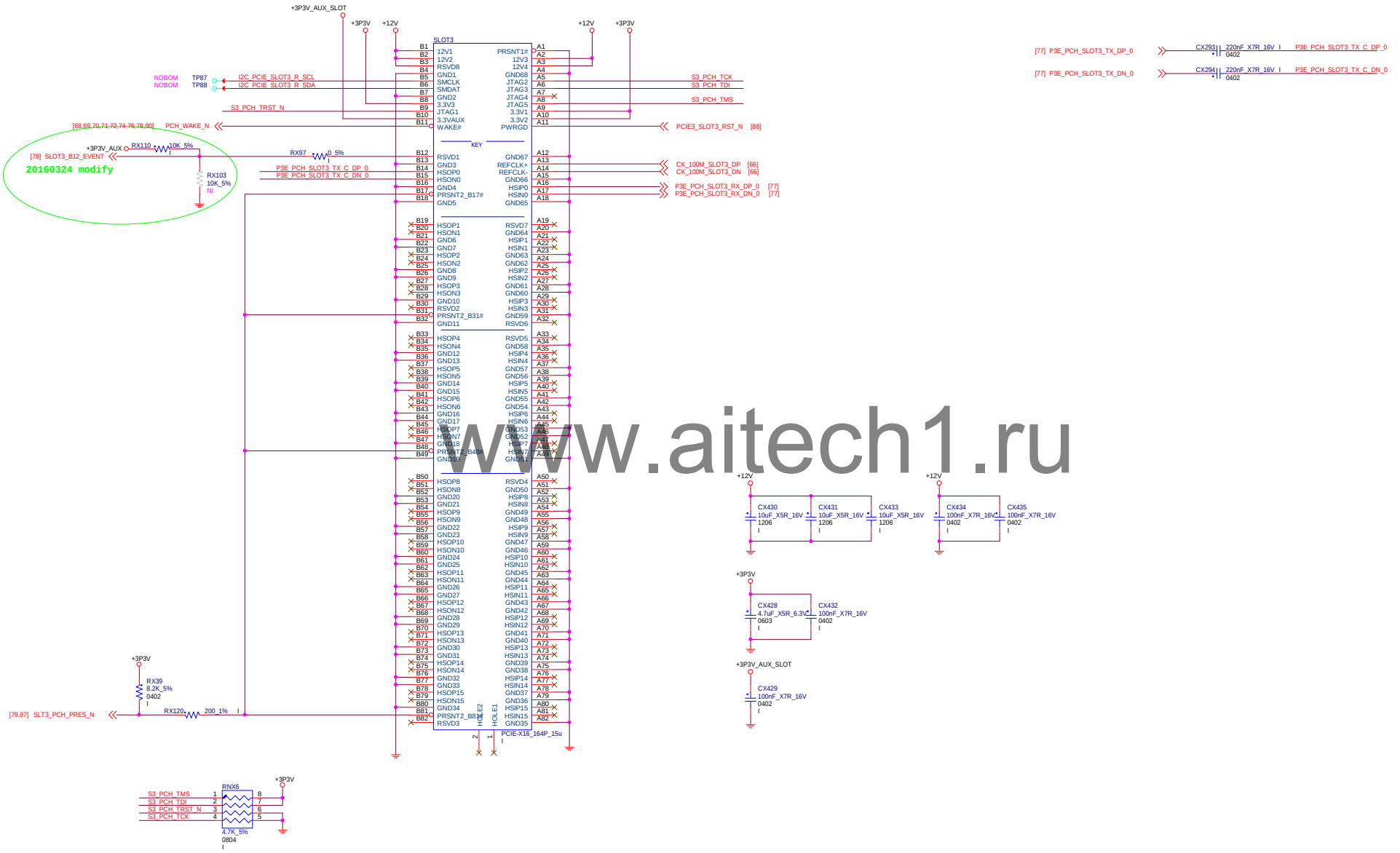
COMPRESSED IMAGE

PCIE x4 SLOT3 (PCH WIRED 1X GEN3)



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TITLE	PCIE G3 X4-Slot3_PCH_1x
DWG NO.	MATIRA 7
REV.	A00
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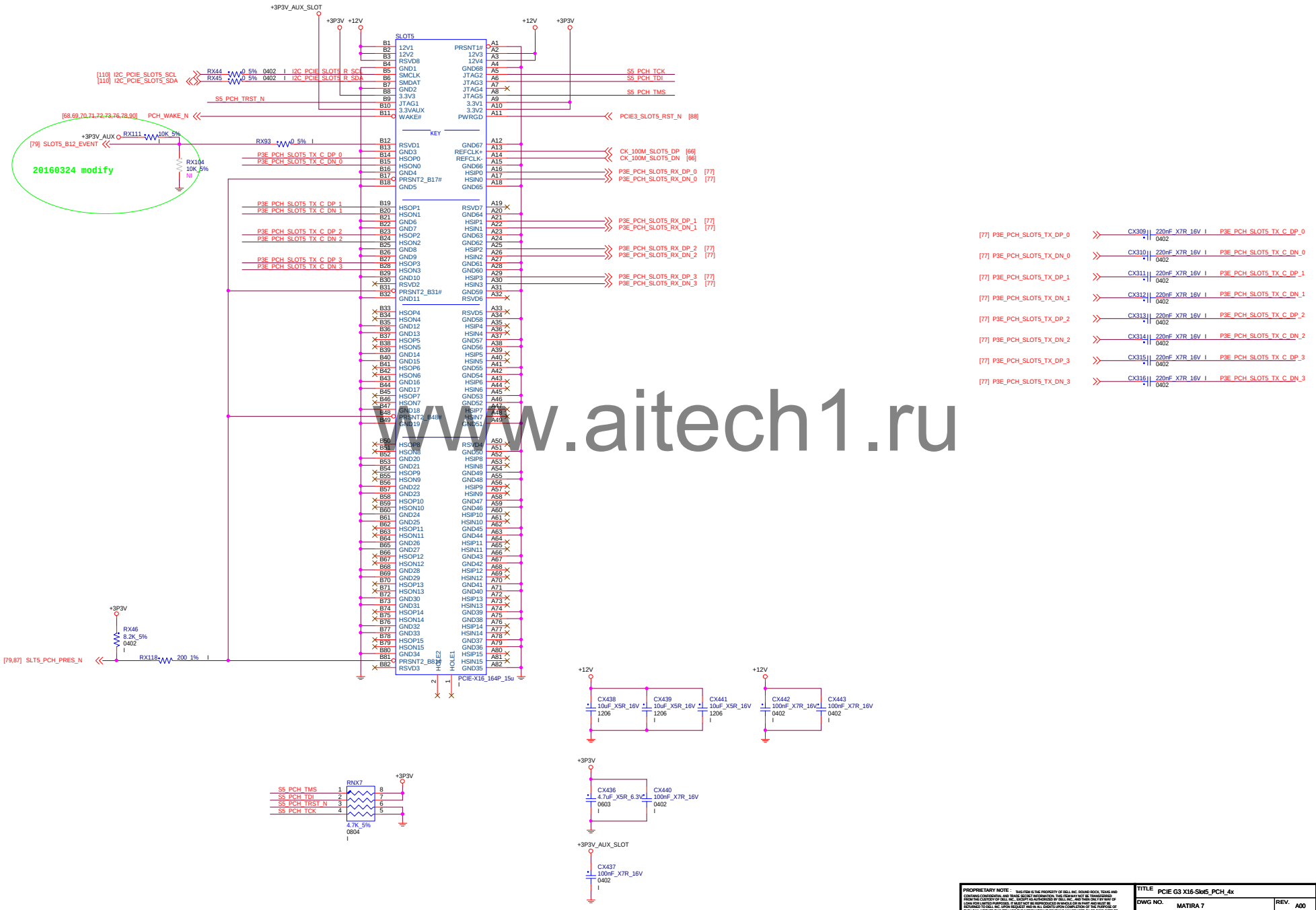
COMPRESSED IMAGE

PCIE x16 SLOT5 (PCH WIRED 4X GEN3)



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TITLE	PCIE G3 X16-Slot5_PCH_4x
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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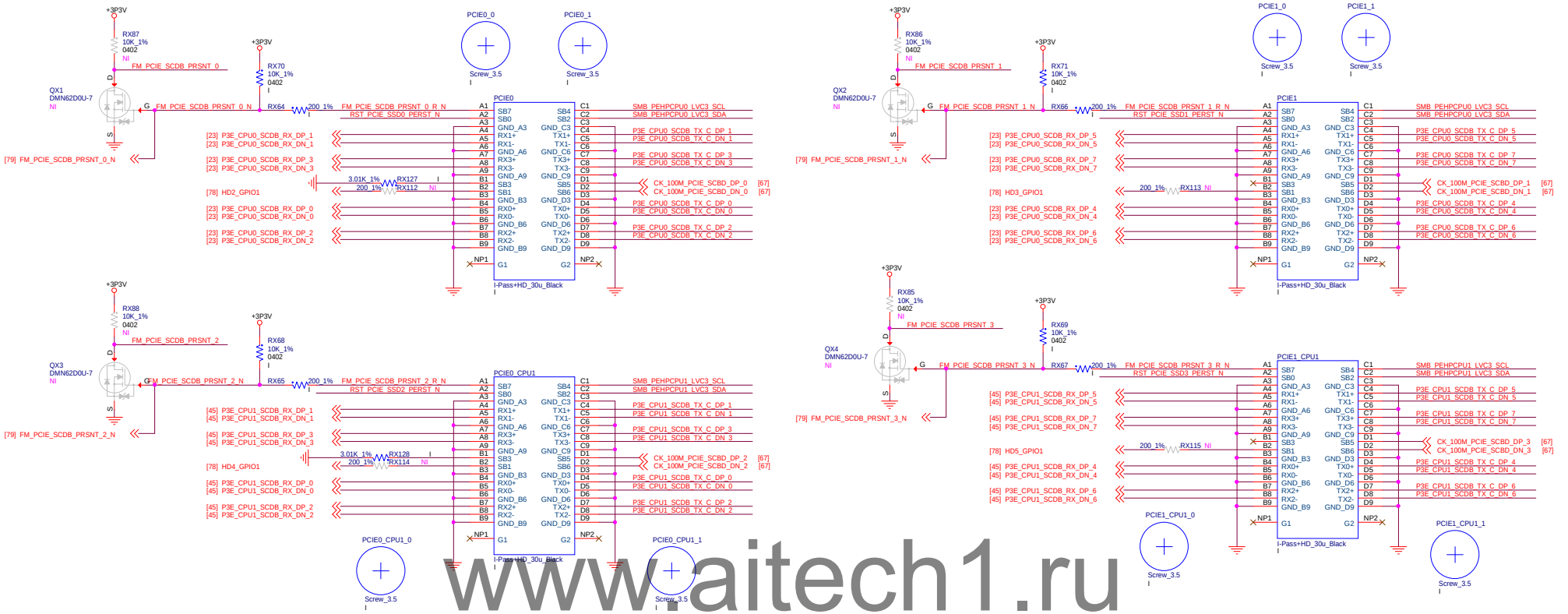
COMPESSED IMAGE

CPU PCIE Storage Connector



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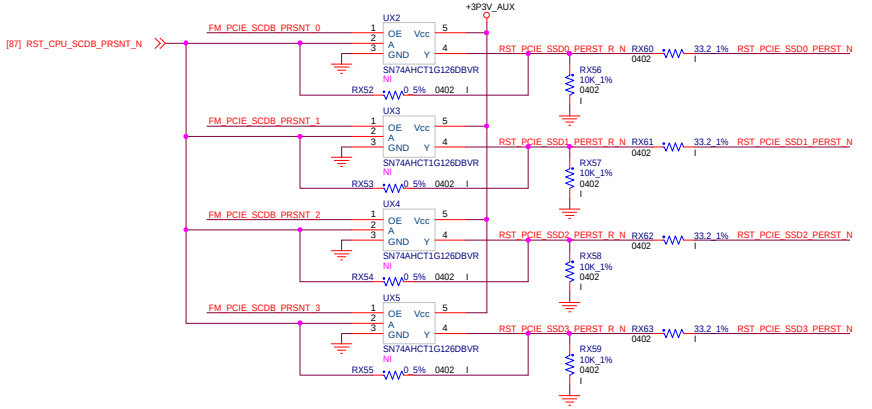
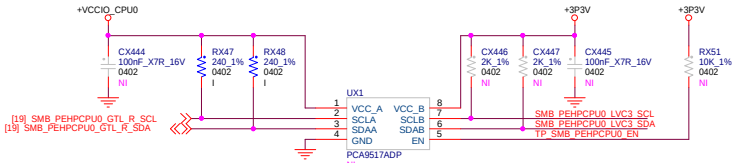


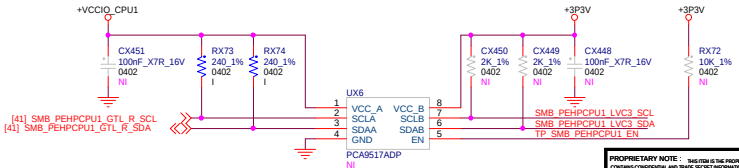
SMB_PEHPCPU0_GTL_R_SCL RX123 0_5% 0402 SMB_PEHPCPU0_LVC3_SCL
SMB_PEHPCPU0_GTL_R_SDA RX124 0_5% 0402 SMB_PEHPCPU0_LVC3_SDA

20160711 modify



SMB_PEHPCPU1_GTL_R_SCL RX125 0_5% 0402 SMB_PEHPCPU1_LVC3_SCL
SMB_PEHPCPU1_GTL_R_SDA RX126 0_5% 0402 SMB_PEHPCPU1_LVC3_SDA

20160711 modify



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TITLE	PCIE Storage Connector
DWG NO.	MATIRA 7
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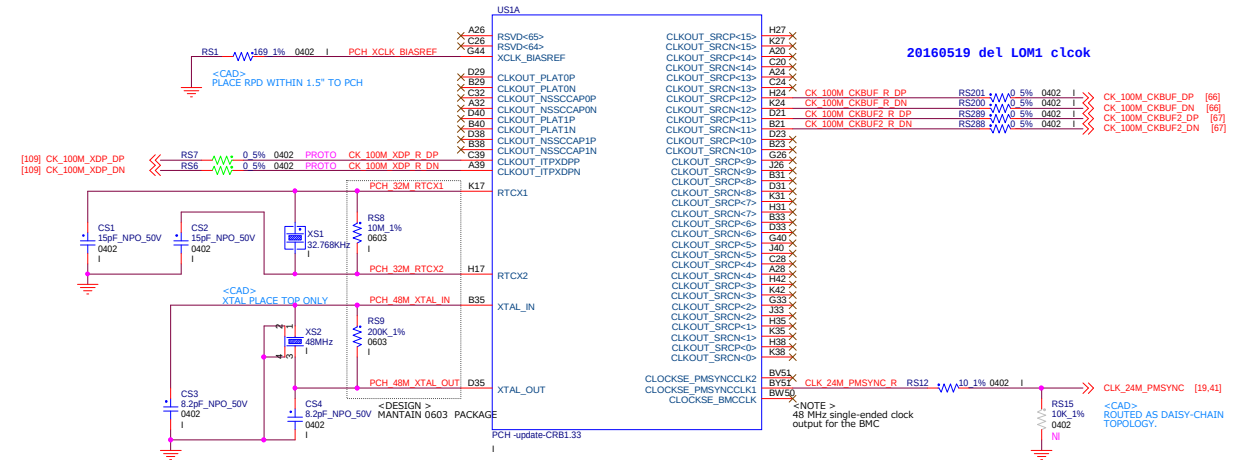
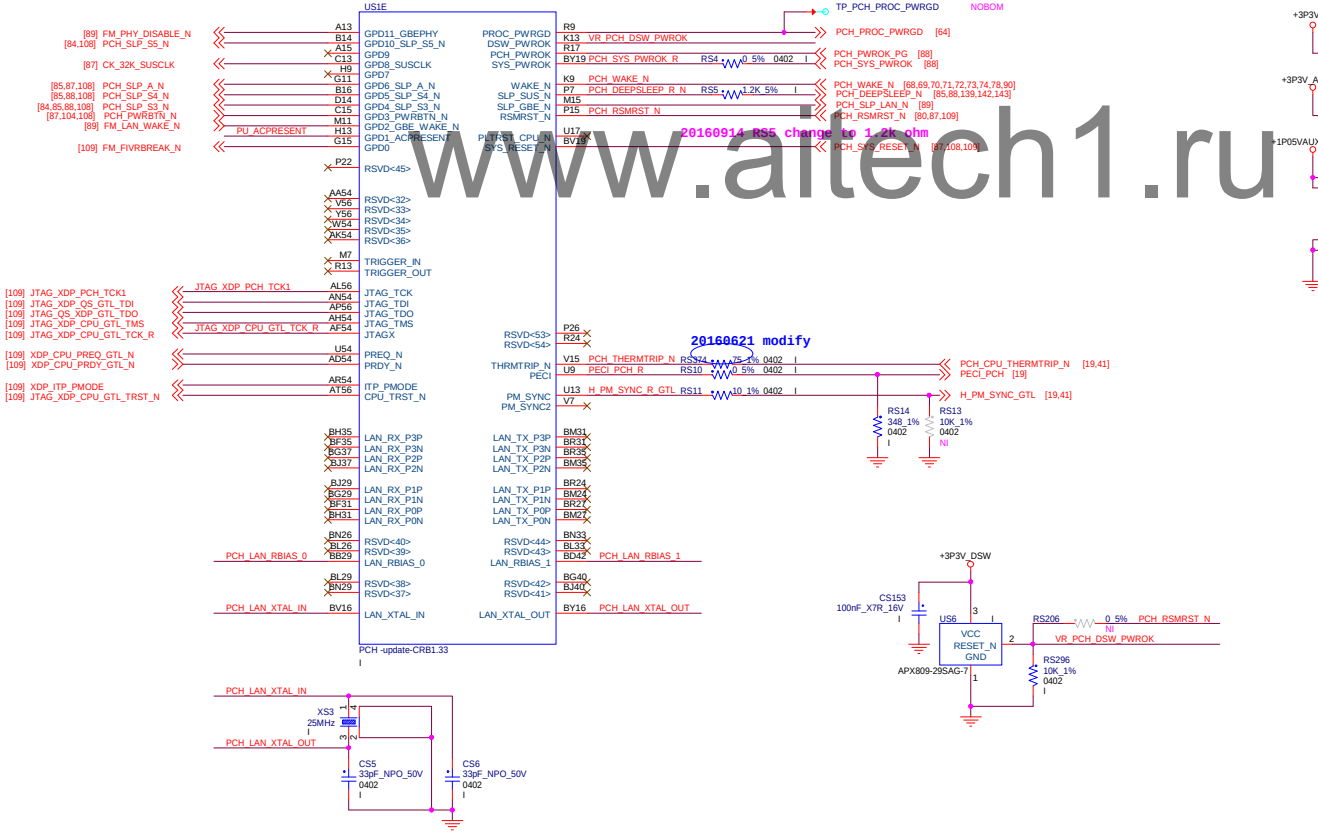


20161115 Modify CS1,CS2,CS3,CS4 value



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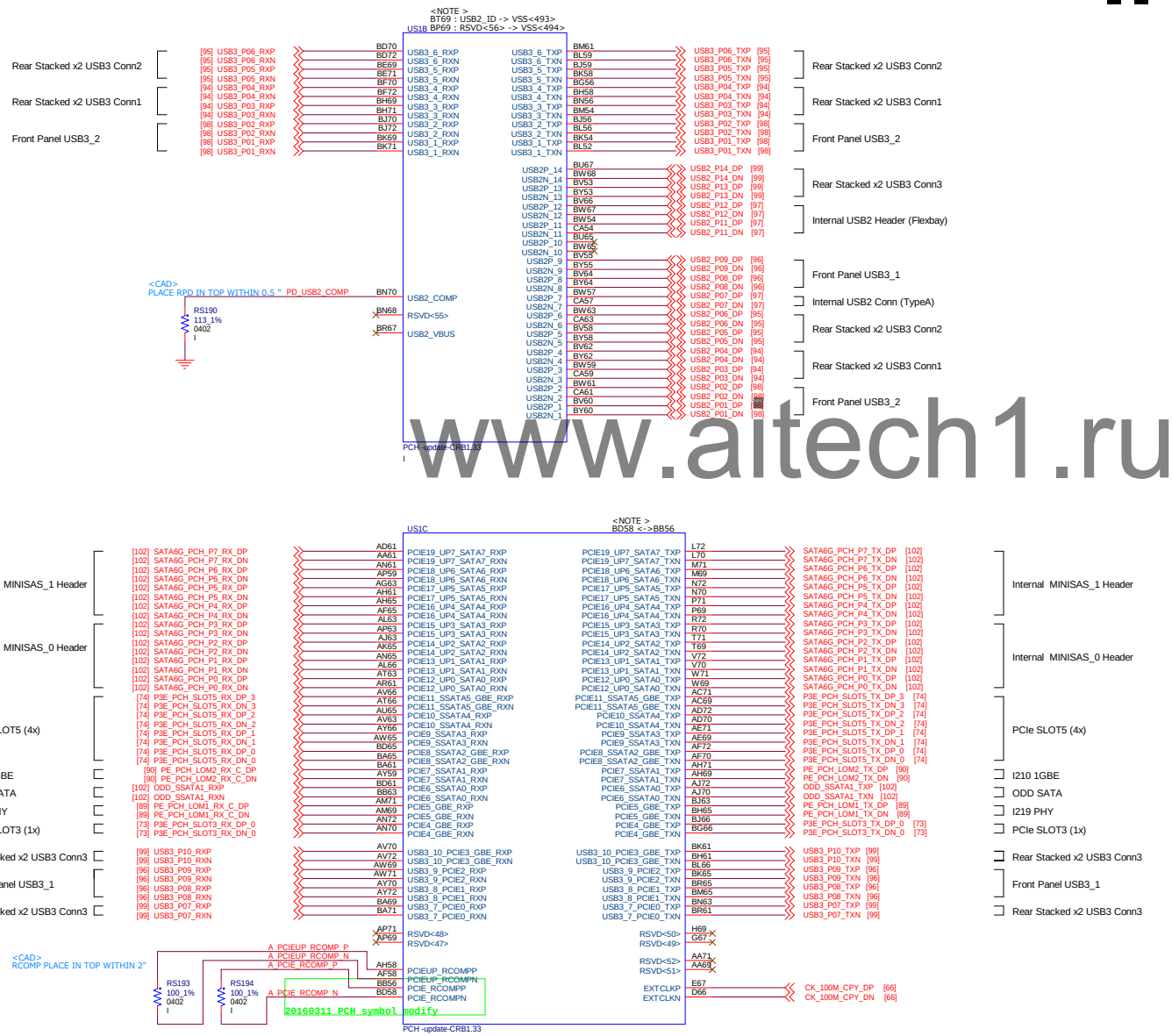

USB Port Mapping Table

USB3	USB2	OC#	Location
1-2	1-2	1	Front Panel USB3_2 (Type C)
3-4	3-4	2	Rear Stacked x2 USB3 Conn1
5-6	5-6	4-5	Rear Stacked x2 USB3 Conn2
	7	6	Internal USB2 Conn (TypeA)
8-9	8-9		Front Panel USB3_1(Hub&SD4.0)
	11-12	7	Internal USB2 Header (Flexbay)
7-10	13-14	3	Rear Stacked x2 USB3 Conn3

SATA Port Mapping Table

SATA3	SSATA3	Location
0-3		Internal_MINISAS_0 Header
4-7		Internal_MINISAS_1 Header

PCIE Port Mapping Table

PCIe3	Function	Location
0	Y	I210 1GBE
1-2		Front USB3 Header
3		I219 1GBE
4	Y	PCIe SLOT 3 (1x)
5	Y	FPIO PCIe SD Card
6	Y	FPIO USB3.1 Controller
7	Y	RPIO USB3.1 Controller
8-11	Y	PCIe SLOT5 (4x)

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+3P3V_AUX
RS131 10K_5% 0402 I GPO_SERVICE_MODE_N

+3P3V_AUX
RS34 1K_1% 0402 I I2C_PCH_3V3STBY_SDA
RS35 1K_1% 0402 I I2C_PCH_3V3STBY_SCL
<CAD> Place Rpu close to PCH within 2"
RS146 10K_5% 0402 I FM_THROTTLE_N

+3P3V_AUX
RS230 1K_1% 0402 I SMB_SMLINK5_STBY_LVC3_SDA
RS231 1K_1% 0402 I SMB_SMLINK5_STBY_LVC3_SCL

USI1D
[63] DMI_CPU0_PCH_TX_C_DP_3 → A45 DMI_RXP<3>
[63] DMI_CPU0_PCH_TX_C_DN_3 → C45 DMI_RXN<3>
[63] DMI_CPU0_PCH_TX_C_DP_2 → B44 DMI_RXP<2>
[63] DMI_CPU0_PCH_TX_C_DN_2 → D44 DMI_RXN<2>
[63] DMI_CPU0_PCH_TX_C_DP_1 → A43 DMI_RXP<1>
[63] DMI_CPU0_PCH_TX_C_DN_1 → C43 DMI_RXN<1>
[63] DMI_CPU0_PCH_TX_C_DP_0 → B42 DMI_RXP<0>
[63] DMI_CPU0_PCH_TX_C_DN_0 → D42 DMI_RXN<0>
DMI_TXP<3> → N54 → DMI_CPU0_PCH_RX_DP_3 [63]
DMI_TXN<3> → P52 → DMI_CPU0_PCH_RX_DN_3 [63]
DMI_TXP<2> → M52 → DMI_CPU0_PCH_RX_DP_2 [63]
DMI_TXN<2> → K50 → DMI_CPU0_PCH_RX_DN_2 [63]
DMI_TXP<1> → J48 → DMI_CPU0_PCH_RX_DP_1 [63]
DMI_TXN<1> → K46 → DMI_CPU0_PCH_RX_DN_1 [63]
DMI_TXP<0> → H46 → DMI_CPU0_PCH_RX_DP_0 [63]
B64 PCIEUP_15_RXP
D64 PCIEUP_15_RXN
A63 PCIEUP_14_RXP
C63 PCIEUP_14_RXN
B62 PCIEUP_13_RXP
D62 PCIEUP_13_RXN
A61 PCIEUP_12_RXP
C61 PCIEUP_12_RXN
B60 PCIEUP_11_RXP
D60 PCIEUP_11_RXN
A59 PCIEUP_10_RXP
C59 PCIEUP_10_RXN
B58 PCIEUP_9_RXP
D58 PCIEUP_9_RXN
A57 PCIEUP_8_RXP
C57 PCIEUP_8_RXN
B55 PCIEUP_7_RXP
D55 PCIEUP_7_RXN
A54 PCIEUP_6_RXP
C54 PCIEUP_6_RXN
B53 PCIEUP_5_RXP
D53 PCIEUP_5_RXN
A52 PCIEUP_4_RXP
C52 PCIEUP_4_RXN
B51 PCIEUP_3_RXP
D51 PCIEUP_3_RXN
A50 PCIEUP_2_RXP
C50 PCIEUP_2_RXN
B49 PCIEUP_1_RXP
D49 PCIEUP_1_RXN
A48 PCIEUP_0_RXP
C48 PCIEUP_0_RXN
PCIEUP_15_TXP AA65
PCIEUP_15_TXN Y66
PCIEUP_14_TXP V63
PCIEUP_14_TXN W65
PCIEUP_13_TXP U61
PCIEUP_13_TXN T63
PCIEUP_12_TXP U65
PCIEUP_12_TXN R65
PCIEUP_11_TXP V59
PCIEUP_11_TXN T59
PCIEUP_10_TXP P66
PCIEUP_10_TXN N65
PCIEUP_9_TXP M66
PCIEUP_9_TXN J66
PCIEUP_8_TXP M63
PCIEUP_8_TXN K65
PCIEUP_7_TXP R61
PCIEUP_7_TXN P59
PCIEUP_6_TXP J63
PCIEUP_6_TXN H61
PCIEUP_5_TXP K61
PCIEUP_5_TXN N61
PCIEUP_4_TXP M59
PCIEUP_4_TXN N58
PCIEUP_3_TXP K58
PCIEUP_3_TXN J56
PCIEUP_2_TXP G56
PCIEUP_2_TXN H54
PCIEUP_1_TXP M56
PCIEUP_1_TXN P56
PCIEUP_0_TXP G52
PCIEUP_0_TXN J52
PCH -update-CRB1.33

+PGPPA_AUX_PCH
RS24 10K_5% 0402 NI PCH_SUSACK_N
RS26 10K_5% 0402 NI PCH_SUSWARN_N
RS28 10K_5% 0402 I IRQ_LPC_SERIRQ_ESPI_CS1_N
RS151 1K_1% 0402 I IRQ_LPC_PIRQA_N_ESPI_ALERT0_N
RS23 1K_1% 0402 I LPC_RCIN_N_ESPI_ALERT1_N
RS266 10K_5% 0402 I FM_LPC_PME_N
RS29 10K_5% 0402 I FM_LPC_CLKRUN_N
RS267 10K_5% 0402 I IRQ_PCH_SCI_WHEA_N

<DESIGN>
SUSACK# and SUSWARN# can be tied together
if EC does not want to involve in the handshake mechanism for
the Deep Sleep state entry and exit.
PCH_SUSACK_N RS27 0_5% 0402 PCH_SUSWARN_N
NI
20170323 modify RS27 to NI from I

CK_24M_66M_MVU_R
CK_24M_66M_EC_R
CK_24M_66M_LEGACY_R
RF485 402_1% 0402 NI
RF486 402_1% 0402 NI
RF487 402_1% 0402 NI
RF41 33_5% 0402 I → CK_24M_66M_MVU [87]
RF92 33_5% 0402 I → CK_24M_66M_EC [85]
RS8 33_5% 0402 NI → CK_24M_66M_LEGACY [108]
RS472 33_5% 0402 I → CK_24M_66M_TCM [107]
RS479 33_5% 0402 I → CK_24M_66M_TPM [107]
20170316 add RF485,RF486,RF487
20170324 depop RF485,RF486,RF487
CF25 100nF_X7R_16V 0402 NI
CF30 100nF_X7R_16V 0402 NI
CF26 100nF_X7R_16V 0402 NI
CF107 100nF_X7R_16V 0402 NI
CF108 100nF_X7R_16V 0402 NI
Reserved for EMI solution
20160901 add RF472,CF107
20160920 add RF479,CF108

USI1F
V1 GPP_A23
AE4 GPP_A22
AE2 GPP_A21
W4 GPP_A20
V3 GPP_A19
AD3 GPP_A18
AD1 GPP_A17
T2 GPP_A16_CLKOUT_LPC2
AC4 GPP_A15_SUSACK_N
AB3 GPP_A14_ESPI_RESET_N
T4 GPP_A13_SUSWARN_N_SUSPWRDNACK
R1 GPP_A12_BMBUSY_N_SXEXITHLDOFF_N
AC2 GPP_A11_PME_N
AA4 GPP_A10_CLKOUT_LPC1
R3 GPP_A9_CLKOUT_LPC0_ESPI_CLK
AB1 GPP_A8_CLKRUN_N
AA2 GPP_A7_PIRQA_N_ESPI_ALERT0_N
P2 GPP_A6_SERIRQ_ESPI_CS1_N
P4 GPP_A5_LFRAME_N_ESPI_CS0_N
V1 GPP_A4_LAD3_ESPI_IO3
W2 GPP_A3_LAD2_ESPI_IO2
N1 GPP_A2_LAD1_ESPI_IO1
Y3 GPP_A1_LAD0_ESPI_IO0
N3 GPP_A0_RCIN_N_ESPI_ALERT1_N
BM20 GPP_B23_MEIE_SML1ALRT_N_PHOT_N
BR17 GPP_B22
BH17 GPP_B21
BJ22 GPP_B20
BK20 GPP_B19
BL15 GPP_B18
BG15 GPP_B17
BG22 GPP_B16
BK13 GPP_B15
BH13 GPP_B14_SPKR
BN18 GPP_B13_PLTRST_N
BL18 GPP_B12_GLB_RST_WARN_N
BK9 GPP_B11
BL11 GPP_B10_SRCCLKREQ5_N
BH20 GPP_B9_SRCCLKREQ4_N
BN11 GPP_B8_SRCCLKREQ3_N
BR13 GPP_B7_SRCCLKREQ2_N
BG18 GPP_B6_SRCCLKREQ1_N
BK17 GPP_B5_SRCCLKREQ0_N
BN7 GPP_B4_CPU_GP3
BR9 GPP_B3_CPU_GP2
BN15 GPP_B2
BH9 GPP_B1_CORE_VID1
BL7 GPP_B0_CORE_VID0
PCH -update-CRB1.33

GPP_C23 CA37
GPP_C22 CA34
GPP_C21 BY33
GPP_C20 CA39
GPP_C19 BW39
GPP_C18 BY35
GPP_C17 BY31
GPP_C16 BW37
GPP_C15 CA32
GPP_C14 BY38
GPP_C13 BW38
GPP_C12 CA30
GPP_C11 BY32
GPP_C10 BY33
GPP_C9 BY29
GPP_C8 BW32
GPP_C7_SML1DATA_IE BV35
GPP_C6_SML1CLK_IE CA28
GPP_C5_SML0ALERT_IE_N BW34
GPP_C4_SML0DATA_IE BW30
GPP_C3_SML0CLK_IE BV29
GPP_C2_SMBALERT_N BY27
GPP_C1_SMBDATA BW28
GPP_C0_SMBCLK BV35
GPP_D23 BN44
GPP_D22_IE_UART_TX BR46
GPP_D21_IE_UART_RX BV44
GPP_D20 CA48
GPP_D19 CA43
GPP_D18 CA41
GPP_D17 BW48
GPP_D16_SML0BALERT_IE_N BV42
GPP_D15_SSATA_SDATAOUT0 BW43
GPP_D14_SML0BDATA_IE BL44
GPP_D13_SML0BCLK_IE BY44
GPP_D12_SSATA_SDATAOUT1 BN40
GPP_D11_SSATA_DEVSLP5 BV47
GPP_D10_SSATA_DEVSLP4 BV42
GPP_D9_SSATA_DEVSLP3 BR38
GPP_D8 CA45
GPP_D7 BW41
GPP_D6 BV40
GPP_D5 BM42
GPP_D4 BW45
GPP_D3 BJ44
GPP_D2 BK46
GPP_D1 BR42
GPP_D0

<NOTE > CABLE
SM_CAT_ERR_DLY_N [84,87]
GPO_CHAR_CB
FM_THROTTLE_N
GPO_CHAR_SMART_CDP
GPO_AUD_SPK_MUTE_N
GPO_SERVICE_MODE_N
FM_PCH_SATA_RAID_KEY
FM_PASSWORD_CLEAR_N [84]
I2C_SM_PCH_SDA [84,85]
I2C_SM_PCH_SCL [84,85]
PU_PCH_LPC_ESPI_STRAP [83]
I2C_PCH_LOM1_SDA [89]
I2C_PCH_LOM1_SCL [89]
PCH_SMBALERT_N [83,85]
I2C_PCH_3V3STBY_SDA [85,90,109]
I2C_PCH_3V3STBY_SCL [85,90,109]
GPO_SD_WP [104]
MINISAS_HD_0_IFDET# [102]
MINISAS_HD_0_PRSNT# [102]
GPI_AUD_PCSPKDET_N [93]
CS147 100nF_X7R_10V
MINISAS_HD_1_IFDET# [102]
MINISAS_HD_1_PRSNT# [102]
GPP_D15:M5 use it.
SMB_SMLINK5_STBY_LVC3_SDA
SMB_SMLINK5_STBY_LVC3_SCL
PU_PCH_GPP_D_11 RS376 33_1% I FM_CPU1_SKTOCC_LVT3_N [41,87,109] 20160901 add
FM_TBT_FORCE_PWR RS150 33_1% NI FM_TBT_FORCE_PWR_R [84,87]
DIAG_LED4_N [87]
DIAG_LED3_N [87]
DIAG_LED2_N [87]
DIAG_LED1_N [87]
SLOT4_B12_EVENT [70]
FM_TBT_SCI_EVENT [84]
SLOT3_B12_EVENT [73]
SLOT2_B12_EVENT [69]
SLOT1_B12_EVENT [68]

SML1 > EC5105
I2C_SM_PCH_SDA
SML0 > I219
I2C_PCH_LOM1
SMB > LAN2 / EC5105 / XDP
I2C_PCH_3V3STBY

[84] PCH_SKU_KEY
[68,69,70,71,72,73,74,76,90] PCH_WAKE_N
[84] FM_UPI_SLOW_MODE_N
RS363 0_5% NI
CK_24M_66M_LEGACY_R
PCH_SUSACK_N
[88] PCH_SUSACK_N
[85,87,108] RST_ESPI_RESET_N
[88] PCH_SUSWARN_N
PCH_SUSWARN_N
IRQ_PCH_SCI_WHEA_N
FM_LPC_PME_N
CK_24M_66M_MVU_R
CK_24M_66M_EC_R
FM_LPC_CLKRUN_N
[85] FM_LPC_CLKRUN_N
[85,87,108] IRQ_LPC_PIRQA_N_ESPI_ALERT0_N
[85,87,107,108] IRQ_LPC_SERIRQ_ESPI_CS1_N
[85,87,107,108] LPC_LFRAME_N_ESPI_CS0_N
[85,87,107,108] LPC_LAD3_ESPI_IO3
[85,87,107,108] LPC_LAD2_ESPI_IO2
[85,87,107,108] LPC_LAD1_ESPI_IO1
[85,87,107,108] LPC_LAD0_ESPI_IO0
[85,87,108] LPC_RCIN_N_ESPI_ALERT1_N
LPC_RCIN_N_ESPI_ALERT1_N
FM_PCH_THERMTRIP_N
[83] FM_PCH_BOOT_BIOS_DEVICE
[93] GPI_AUD_CABLE_N
20160517 Add
[64,87] FM_CPU_ERR0_LVT3_N
[83] PU_NO_REBOOT
SM_ERROR_OUT_R_N
[64,87] FM_CPU_ERR1_LVT3_N
[64,87] FM_CPU_ERR0_LVT3_N
[83] FM_PCH_BIOS_RCVR_SPKR
[78,85,88,108] PCH_PLTRST_N
[95] USBPWR_6_7_EN
[104] HDD_TEMP_DET1#
[104] HDD_TEMP_DET2#
[84] GPI_TBT_CABLE_N
[75] HD5_GPIO1
[75] HD4_GPIO1
[75] HD3_GPIO1
[75] HD2_GPIO1
HDD_TEMP_DET1#
HDD_TEMP_DET2#
GPI_TBT_CABLE_N
HD5_GPIO1
HD4_GPIO1
HD3_GPIO1
HD2_GPIO1
RS294 10K_5%
RS295 10K_5%
+3P3V_AUX
PCH_CORE_VID_1
PCH_CORE_VID_0
B8,B10 M5 use
to CLKREQ
20160426 modify
[87] SM_ERROR_OUT_N
RS258 0_5% 0402 I SM_ERROR_OUT_R_N

DOUBLE CHECK AGAIN
FOLLOW CRB

[88] PCH_PHOT_N
[78,85,88,108] PCH_PLTRST_N
RS25 10K_5% 0402 I
RS207 1M_1% 0402 I
QS1 DMN62D0U-7
FM_PCH_THERMTRIP_N
RS36 1K_1% 0402 I
RS37 1K_1% 0402 I
QS2 DMN62D0U-7
QS3 DMN62D0U-7
I2C_PCH_3V3STBY_SDA
I2C_PCH_3V3STBY_SCL
I2C_PCH_3V3_SDA [66,67,102]
I2C_PCH_3V3_SCL [66,67,102]
AUX_FROM_MAIN_12V [104,143]
FOR CLOCK BUFFER
RPU FOLLOW A7 4.7K > 1K

PCH PULLUPS / PULLDOWNS

+3P3V_AUX
RS264 10K_5% NI GPO_AUD_SPK_MUTE_N

+3P3V_AUX
RS216 10K_5% 0402 I GPO_CHAR_SMART_CDP
RS217 10K_5% 0402 I GPO_CHAR_CB
RS222 10K_5% 0402 NI PU_PCH_GPP_D_11
RS215 10K_5% 0402 I HD2_GPIO1
RS214 10K_5% 0402 I HD3_GPIO1
RS298 10K_5% 0402 I HD4_GPIO1

+3P3V_AUX
RS280 10K_5% 0402 I HDD_TEMP_DET2#
RS281 10K_5% 0402 I HDD_TEMP_DET1#
RS282 10K_5% 0402 I GPI_TBT_CABLE_N
RS283 10K_5% 0402 I HD5_GPIO1

RS101 10K_5% NI FM_TBT_FORCE_PWR
RS102 10K_5% NI FM_TBT_SCI_EVENT
I 10K_5% RS362 +3P3V_AUX

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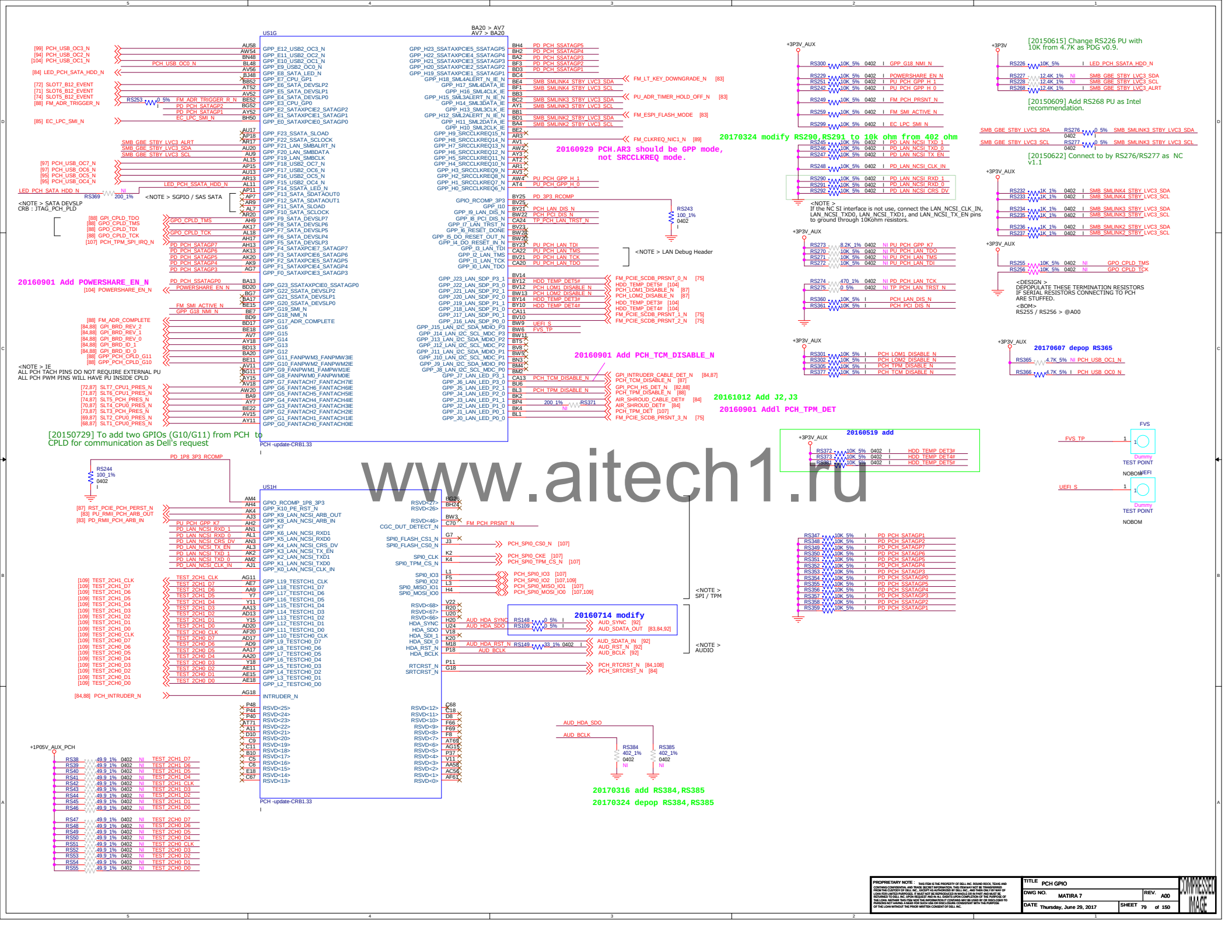

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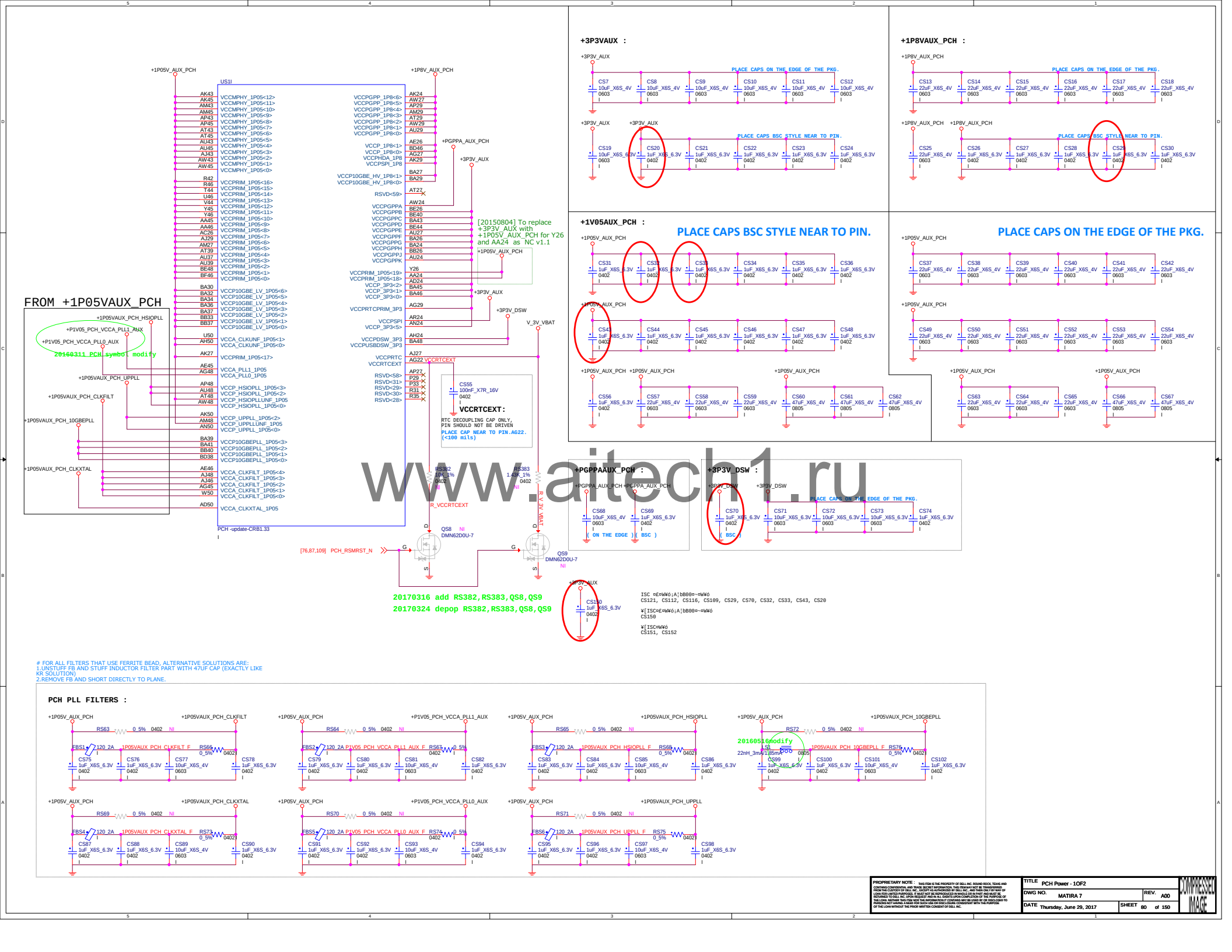

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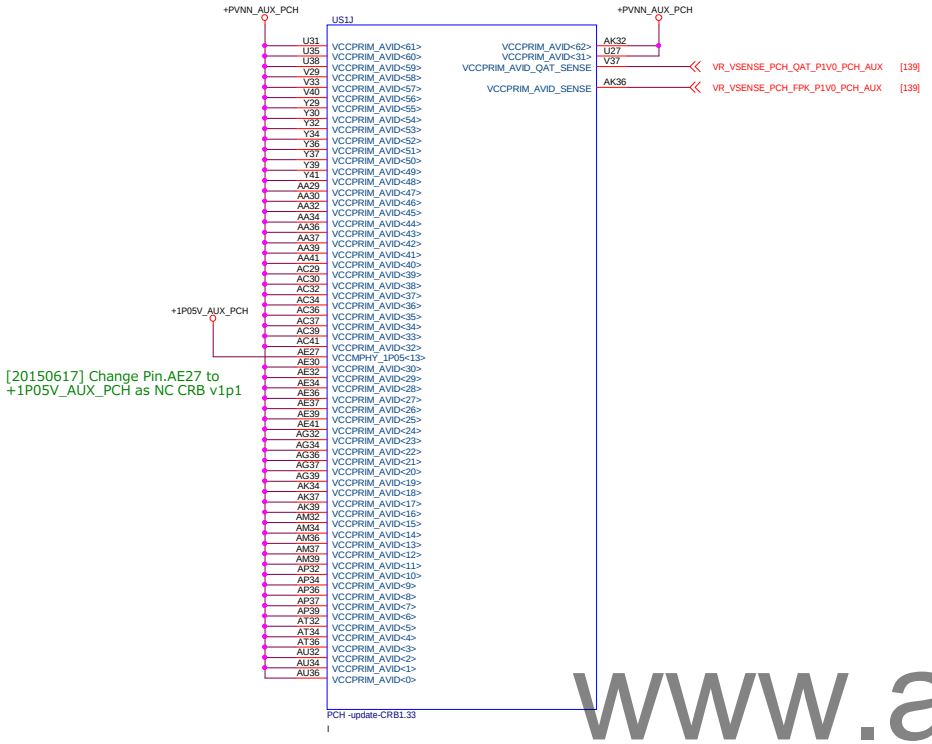

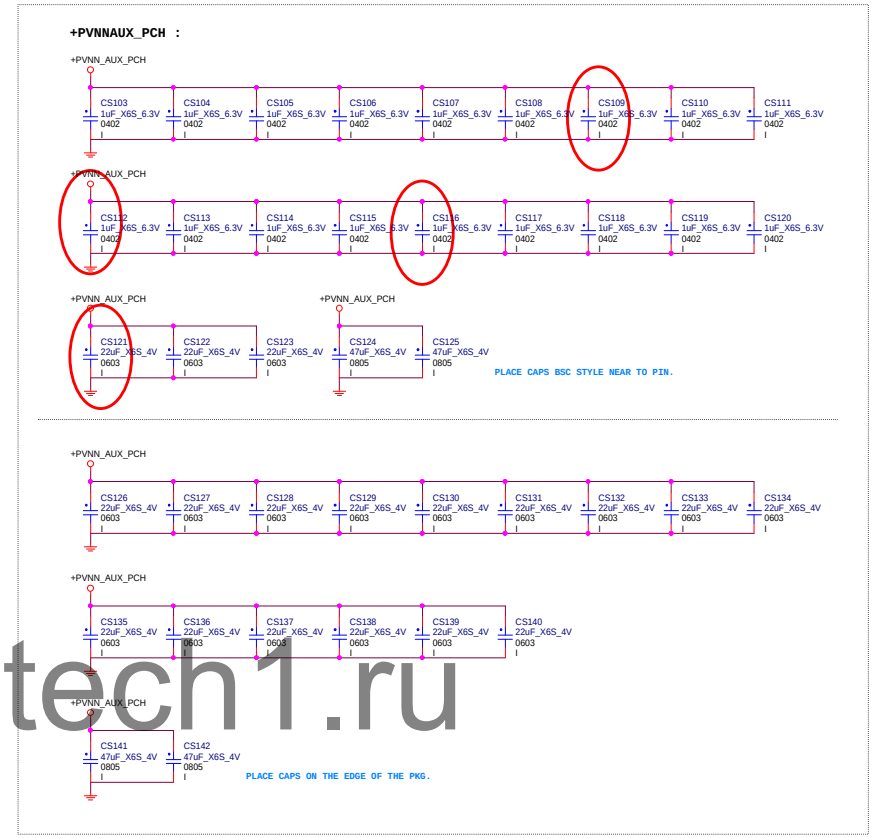

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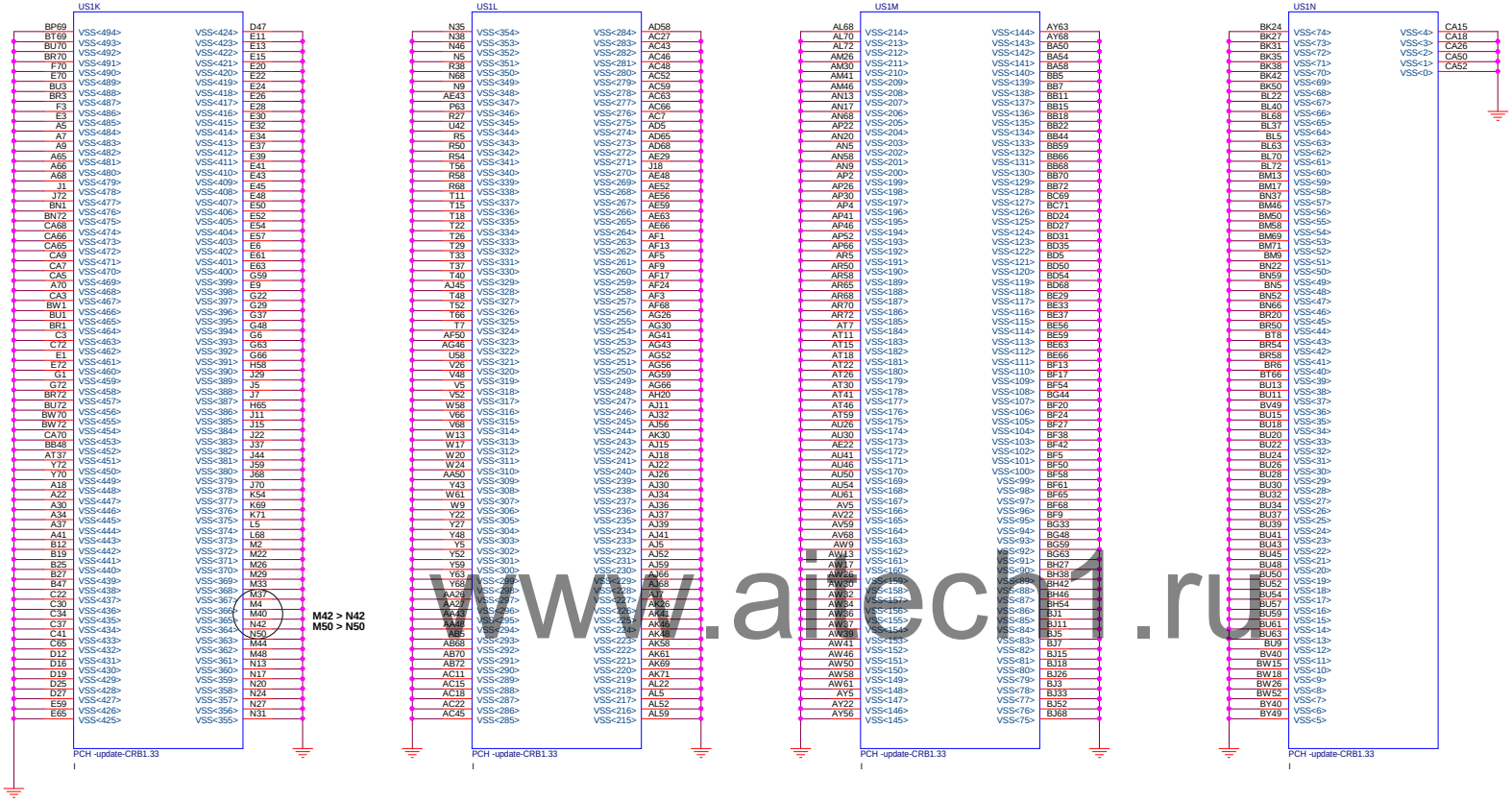
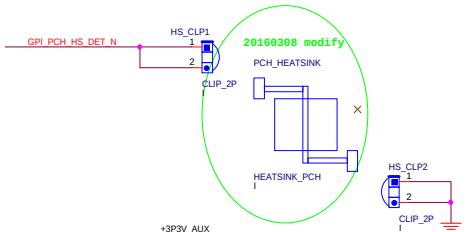
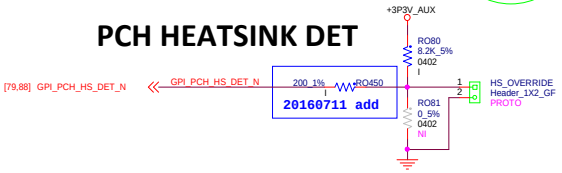
COMPRESSED IMAGE





PCH HEATSINK DET



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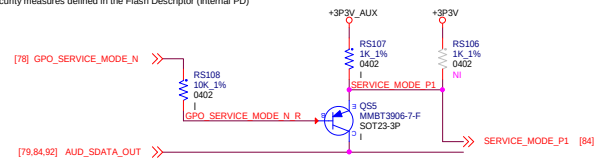
COMPRESSED IMAGE

SERVICE MODE JUMPER

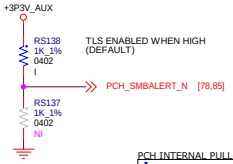
(ME FW Override Jumper)
1 : Disable Flash Descriptor Security (Override)
0 : Enable security measures defined in the Flash Descriptor (Internal PD)

FLASH SECURITY OVERRIDE
PCH INTERNAL PULL-DOWN.

1 > FLASH SECURITY OVERRIDE ENABLE
0 >FLASH SECURITY OVERRYDE DISABLE (DEFAULT)



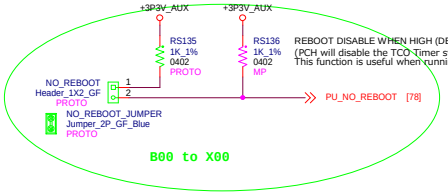
TLS CONFIDENTIALITY



PCH INTERNAL PULL-DOWN.

* 1 > TLS ENABLED
0 >TLS DISABLE

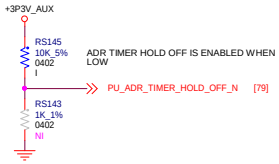
NO REBOOT STRAP



PCH INTERNAL PULL-DOWN.

* 1 > Enable ¡§No Reboot¡¨ mode.
0 > Disable ¡§No Reboot¡¨ mode.

ADR TIMER OFF



PCH INTERNAL PULL-UP

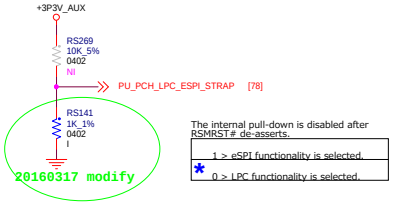
1 > ADR Timer Hold off is not enabled.
0 > ADR Timer Hold off is enabled.

ESPI FLASH SHARING MODE

PCH INTERNAL PULL-DOWN.

1 > SLAVE ESPI FLASH SHARING
0 > MASTER ESPI FLASH SHARING (DEFAULT)

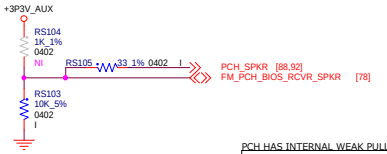
ESPI OR LPC



The internal pull-down is disabled after RSMRST# de-asserts.

1 > eSPI functionality is selected.
* 0 > LPC functionality is selected.

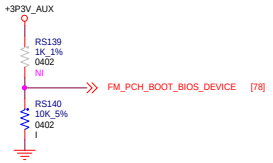
TOP SWAP MODE STRAP



PCH HAS INTERNAL WEAK PULL-DOWN

1 >TOP SWAP ENABLED
0 > TOP SWAP DISABLED (DEFAULT)

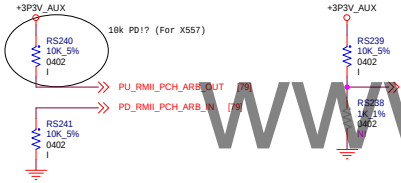
BOOT BIOS DEVICE



PCH INTERNAL PULL-DOWN.

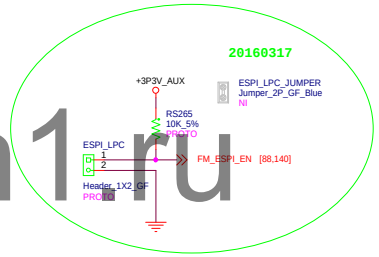
1 > LPC / ESPI
* 0 > SPI (DEFAULT)

D3COLD POWER STATE



PCH INTERNAL PULL-DOWN.

1 > Aux power is available and the 10Gbe LAN should support the D3COLD power state if enabled to do s0.
0 > D3COLD is not supported.



GPPA	FM_ESPI_EN
3.3V	0
1.8V	1

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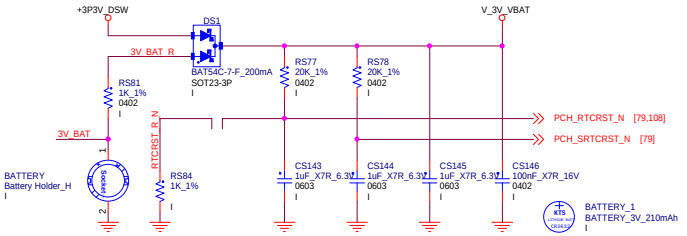
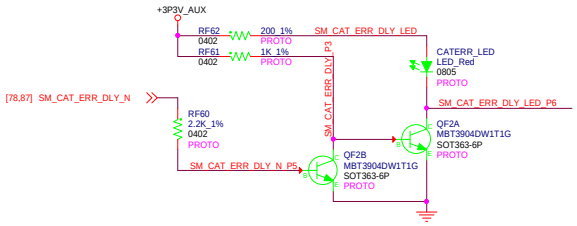
COMPRESSED IMAGE

RTC BATTERY

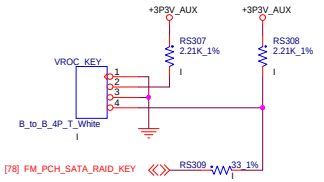


CATERR LED

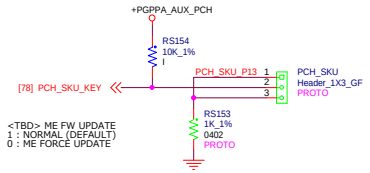


SATA RAID KEY

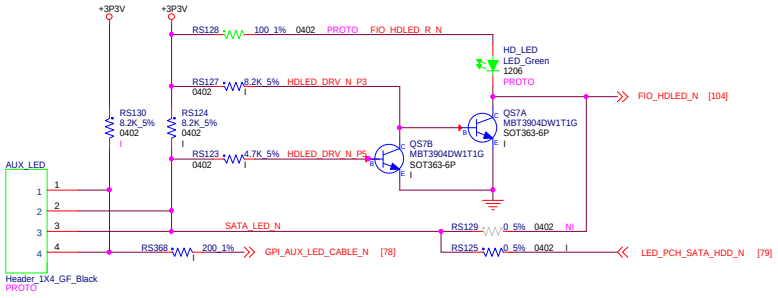
20161014 modify VROC_KEY material



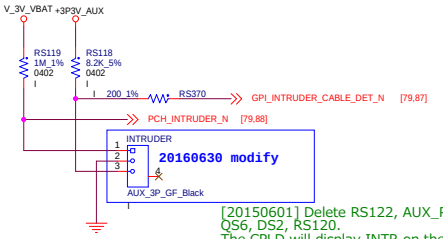
PCH KEY



AUX LED

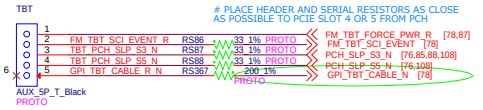


INTRUDER DECTECTION SWITCH



[201506011 Delete RS122, AUX_PWR, RS121, QS6, DS2, RS120.
The CPLD will display INTR on the onboard display when INTRUDER is detected. No need for this external LED circuitry.

THUNDERBOLT SIDEBAND



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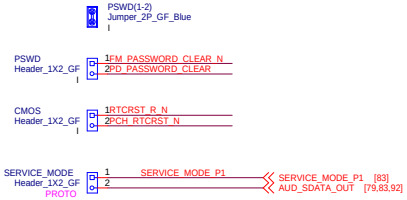
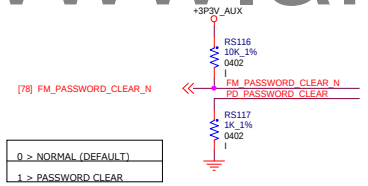
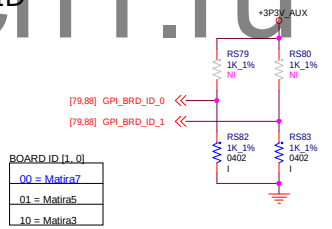
PASSWORD JUMPER

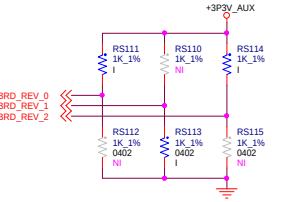




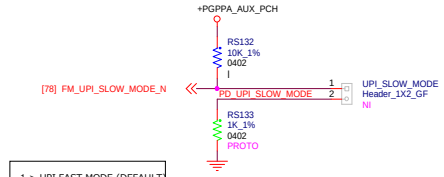
BOARD ID



BOARD REVISION ID

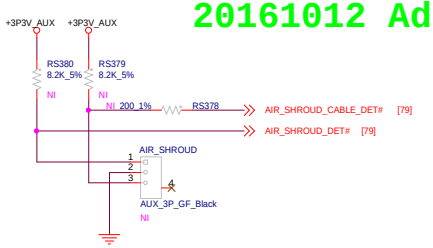


UPI SLOW MODE

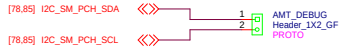


Air Shroud Dectection Switch

20161012 Add



AMT DEBUG HOOK



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TITLE	Miscellaneous
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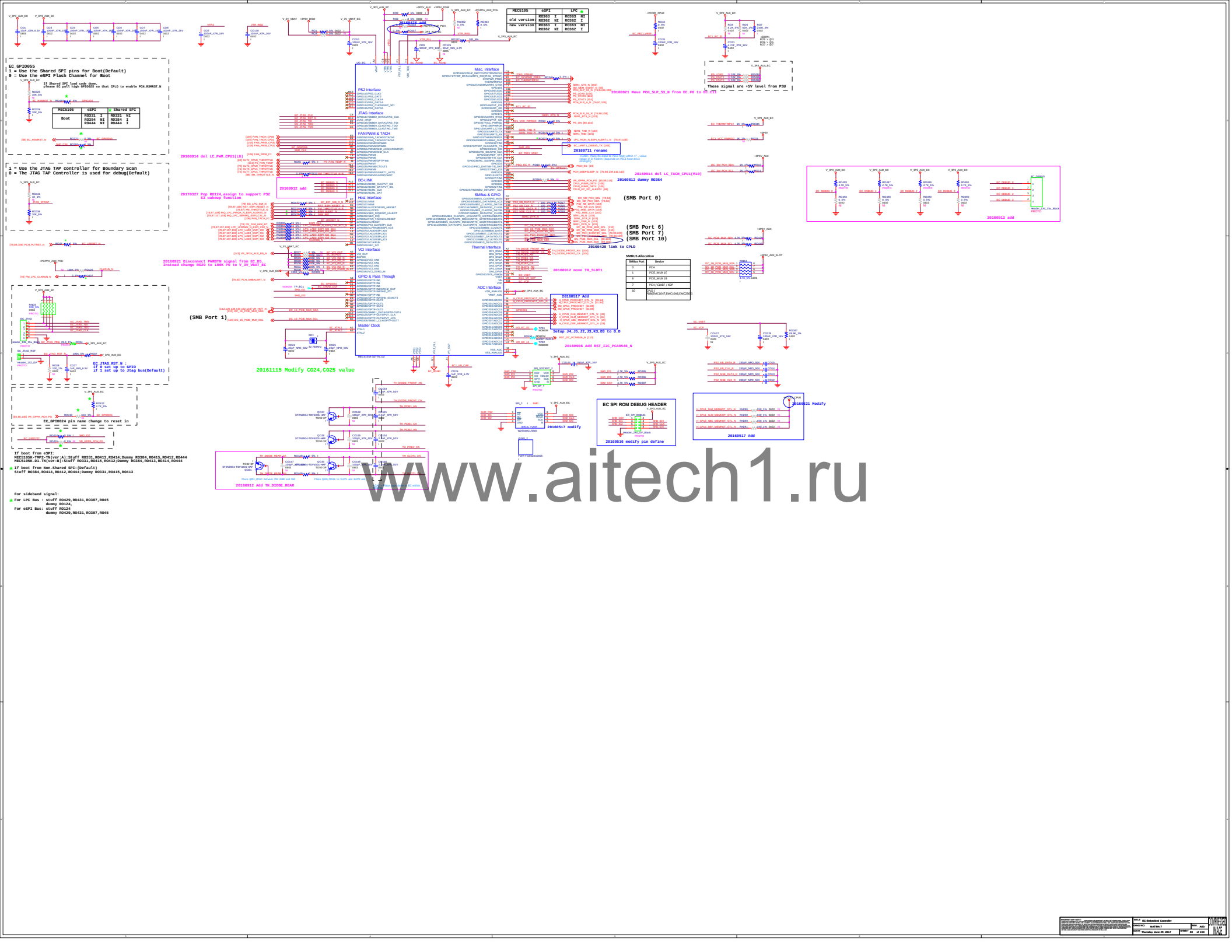
COMPOSED IMAGE



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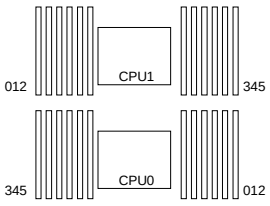
20160308 del



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TITLE	EC GPIO Expander		
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COMPRESSED IMAGE

[78,85,107,108] LPC_LFRAME_N_ESPI_CS0_N
[78,85,107,108] IRQ_LPC_SERIRQ_ESPI_CS1_N
RO284 0_5% I
RO430 0_5% NI
LPC_LFRAME_N_ESPI_CS0_CPLD_N

20160914 Add G6,H1,J3,J4,J5,K2,K6,L10

UO1A I

[78,85] FM_THROTTLE_N
[64,78] FM_CPU_ERR0_LVT3_N
[79] RST_PCIE_PCH_PERST_N
[66,67] CPLD_CKBUF_EN
[78,84] SM_CAT_ERR_DLY_N
[89] LOM1_RST_N
[140] VR_1P8V_GPPA_PCH_EN
[64,78] FM_CPU_ERR1_LVT3_N
[76] CK_32K_SUSCLK
[19] FM_CPU0_PKGID0
[106] FAN_PWM_F2
[19] FM_CPU0_PROC_ID1
[19] FM_CPU0_PROC_ID0
[76,108,109] PCH_SYS_RESET_N
[76,80,109] PCH_RSMRST_N
[19] FM_CPU0_PKGID2
[19] FM_CPU0_PKGID1
[90] LOM2_RST_N
[141] VR_3P3_5V_PG
[78,85,107,108] LPC_LAD0_ESPI_IO0
[78,85,107,108] LPC_LAD1_ESPI_IO1
[78,85,107,108] LPC_LAD2_ESPI_IO2
[78,85,107,108] LPC_LAD3_ESPI_IO3
LPC_LFRAME_N_ESPI_CS0_CPLD_N
[106] FAN_PWM_F3
[78] CK_24M_66M_MVU
[106] FAN_PWM_F4
[78,85,108] IRQ_LPC_PIRQA_N_ESPI_ALERT0_N
[78,85,108] LPC_RCIN_N_ESPI_ALERT1_N
[78,85,108] RST_ESPI_RESET_N
[106] FAN_TACH_F4
[106] FAN_TACH_R1
[106] FAN_PWM_R1
[106] FAN_PWM_R2
[112] VR_CPU0_VCCSA_PG
[138] VR_MEM_VTT_DRVR_CPU1_EN
[78] SM_ERROR_OUT_N
[19] PWRGD_CPU0_GTL
[112] VR_CPU0_VCCIN_PG
[142] VR_3P3V_AUX_SLOT_EN
[104] POWER2_PRES
[64,78] FM_CPU_ERR2_LVT3_N
[75] RST_CPU_SCDB_PRSNT_N
[120] VR_CPU1_VCCIN_PG
[134] VR_MEM345_VDD_CPU1_PG
[104] POWER2B_PRES
[132] VR_MEM012_VDD_CPU1_PG
[102] MINISAS_HD_0_RST
[104] PWRLED_AMBER_N
[104] PWRLED_WHITE_N

RO239 0_5% 0402 I LOM1_BFR_RST_N
VR_1P8V_GPPA_PCH_EN
RO160 0_5% 0402 CK_32K_SUSCLK_CPLD
PROTO
RO361 0_5% I
RO315 0_5% 0402 I LOM2_BFR_RST_N
RO276 0_5% 0402 I LPC_LAD0_ESPI_IO0_CPLD
RO277 0_5% 0402 I LPC_LAD0_ESPI_IO1_CPLD
RO278 0_5% 0402 I LPC_LAD0_ESPI_IO2_CPLD
RO279 0_5% 0402 I LPC_LAD0_ESPI_IO3_CPLD
FAN_TACH_F4
FAN_TACH_R1
VR_MEM_VTT_DRVR_CPU1_EN
VR_3P3V_AUX_SLOT_EN
RO235 0_5% 0402 I CPU_SCBD_BFR_RST_N

D3 PL1A/L_GPLLT_FB
D1 PL1B/L_GPLLC_FB
B1 PL1C
C2 PL1D
E2 PL2A/L_GPLLT_IN
E3 PL2B/L_GPLLC_IN
C1 PL2C
D2 PL2D
E1 PL3A/PCLKT5_0
F2 PL3B/PCLKC5_0
F4 PL3C
G6 PL3D
F3 PL4A
F1 PL4B
G5 PL4C
G4 PL4D
G2 PL5A
G3 PL5B
F5 PL5C
H6 PL5D
G1 PL6A
H2 PL6B
H4 PL6C
J6 PL6D
H3 PL7A
H1 PL7B
J1 PL7C/PCLKT4_0
J3 PL7D/PCLKC4_0
J2 PL9A
K1 PL9B
H5 PL9C
J4 PL9D
K3 PL10A
K2 PL10B
J5 PL10C
K6 PL10D
L1 PL11A
L3 PL11B
K4 PL11C
L5 PL11D
L2 PL12A/PCLKT3_0
M1 PL12B/PCLKC3_0
K5 PL12C
L4 PL12D
M3 PL13A
M5 PL13B
N2 PL13C
P1 PL13D
M2 PL14A
N3 PL14B
R1 PL14C
P2 PL14D

BANK5
BANK4
BANK3
BANK2
1/3

P4 PB3A
T4 PB3B
T2 UO1_T2 TP90 NOBOM
R3 PB3C
PB3D
R5 PB5A/CSSPIN
P5 PB5B
T5 UO1_T5 TP89 NOBOM
R6 PB6A
P8 PB6B
T3 PB6C
R4 PB6D
P6 PB8A/MCLK/CCLK
T6 PB8B/SO/SPISO
N6 PB8C
L7 PB8D
R7 PB9A
P7 PB9B
M7 PB9C
N7 PB9D
T7 PB11A/PCLKT2_0
R8 PB11B/PCLKC2_0
M6 PB11C
L8 PB11D
P8 PB12A
T8 PB12B
N8 PB12C
L9 PB12D
T9 PB16A/PCLKT2_1
P9 PB16B/PCLKC2_1
M8 PB16C
N9 PB16D
R9 PB18A
T10 PB18B
M9 PB18C
L10 PB18D
P10 PB19A
R10 PB19B
N10 PB19C
M11 PB19D
T11 PB21A
P11 PB21B
M10 PB21C
N11 PB21D
R11 PB22A
T12 PB22B
R13 PB22C
T14 PB22D
P12 PB24A
T13 PB24B
R12 PB25A/SN
P13 PB25B/SI/SISPI
T15 PB25C
R14 PB25D

VR_CPU1_VCCSA_PG [120]
FM_CPU1_PKGID0 [41]
VR_MEM_VPP_CPU0_EN [136]
VR_MEM_VPP_CPU1_EN [137]
PCH_TCM_DISABLE_N [79]
GPO_LOM2_EN [90]
PCH_LOM2_DISABLE_N [79]
DIAG_LED1_N [78]
DIAG_LED2_N [78]
DIAG_LED3_N [78]
DIAG_LED4_N [78]
VR_MEM345_VDD_CPU0_PG [130]
V_5VAUX_MEM_CPU1_EN_N [143]
VR_CPU0_VCCIO_EN [115]
VR_MEM012_VDD_CPU0_PG [128]
VR_CPU1_VCCIO_EN [123]
SLT4_CPU0_PRES_N [70,79]
FLASH_EN# [107]
VR_CPU0_VCCIO_PG [109,115]
VR_1P05V_PCH_PG [140]
SLT6_CPU1_PRES_N [71,79]
SLT2_CPU0_PRES_N [69,79]
FM_TBT_FORCE_PWR_R [78,84]
PCH_PWRBTN_N [76,104,108]
CPLD_SPEAKER [108]
VR_3P3V_EN [141]
SLT7_CPU1_PRES_N [72,79]
SLT5_PCH_PRES_N [74,79]
SLT1_CPU0_PRES_N [68,79]
SLT3_PCH_PRES_N [73,79]
FAN_TACH_R2 [106]
MINISAS_HD_1_RST [102]
RST_CPU0_GTL_N [19]
RST_CPU1_GTL_N [41]
XDP_PWRGD_RST_N [109]
FM_CPU1_PKGID2 [41]
PCH_SLP_A_N [76,85,108]
PWRGD_CPU1_GTL [41]
CPU_XDP_SYSPWROK [109]
FM_CPU1_SKTOCC_LVT3_N
PU_CPU0_SKTOCC_LVT3_N [19,109]
DU_CPU1_PKGID1 [41]
SM_CPU_MSWI [64]
GPI_INTRUDER_CABLE_DET_N [79,84]
SM_CPU_CATERR [64]

PCH_LOM1_DISABLE_N [79]
UO1_T2 TP90 NOBOM
FM_CPU1_PKGID0 [41]
UO1_T5 TP89 NOBOM
PCH_TCM_DISABLE_N [79]
PCH_LOM2_DISABLE_N [79]
VR_CPU0_VCCIO_EN
VR_CPU1_VCCIO_EN
FLASH_EN#
CPLD_TBT_FORCE_PWR
RO220 33_1% I
PU_PB25A_SN

[20150604] Change FM_CPU1_PKGID0 from PB25A to PB3D as Lattice recommendation.

20160901 Add PCH_TCM_DISABLE_N

20160517 change to O.D
20160517 change to O.D
20160509 del CLK_CPU1_BCLKS_EN_N
20160509 del PCH_FUSB31_DISABLE_N
20160517 modify

[20150604] PU with 4.7K at pin PB25A as Lattice recommendation.

LPC/eSPI Bus

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+3P3V_CPLD

FLASH_EN# RO416 4.7K_5% 0402 I
VR_1P05V_PCH_PG RO145 10K_5% 0402 NI
VR_3P3_5V_PG RO249 10K_5% 0402 NI
PU_PB25A_SN RO301 4.7K_5% 0402 I

FAN_TACH_R1
FAN_TACH_F4
CO150 10nF_X7R_16V I
CO151 10nF_X7R_16V I

@UO1
FWR-FH602D10000
I

VR_1P8V_GPPA_PCH_EN RO163 2K_1% 0402 I
VR_MEM_VTT_DRVR_CPU1_EN RO165 2K_1% 0402 I
VR_CPU0_VCCIO_EN RO172 2K_1% 0402 I
VR_CPU1_VCCIO_EN RO173 2K_1% 0402 I
VR_3P3V_EN RO216 2K_1% 0402 I
VR_3P3V_AUX_SLOT_EN RO214 2K_1% 0402 I

Only CPLD

PROC_ID[1:0]	Definition
00	CNL SKL
01	
10	RESERVED
11	CNL-G

PKG_ID[2:0]	Definition
000	Non-MCP
001	Fabric(-F)
010	FPGA(-P)
111-011	RESERVED

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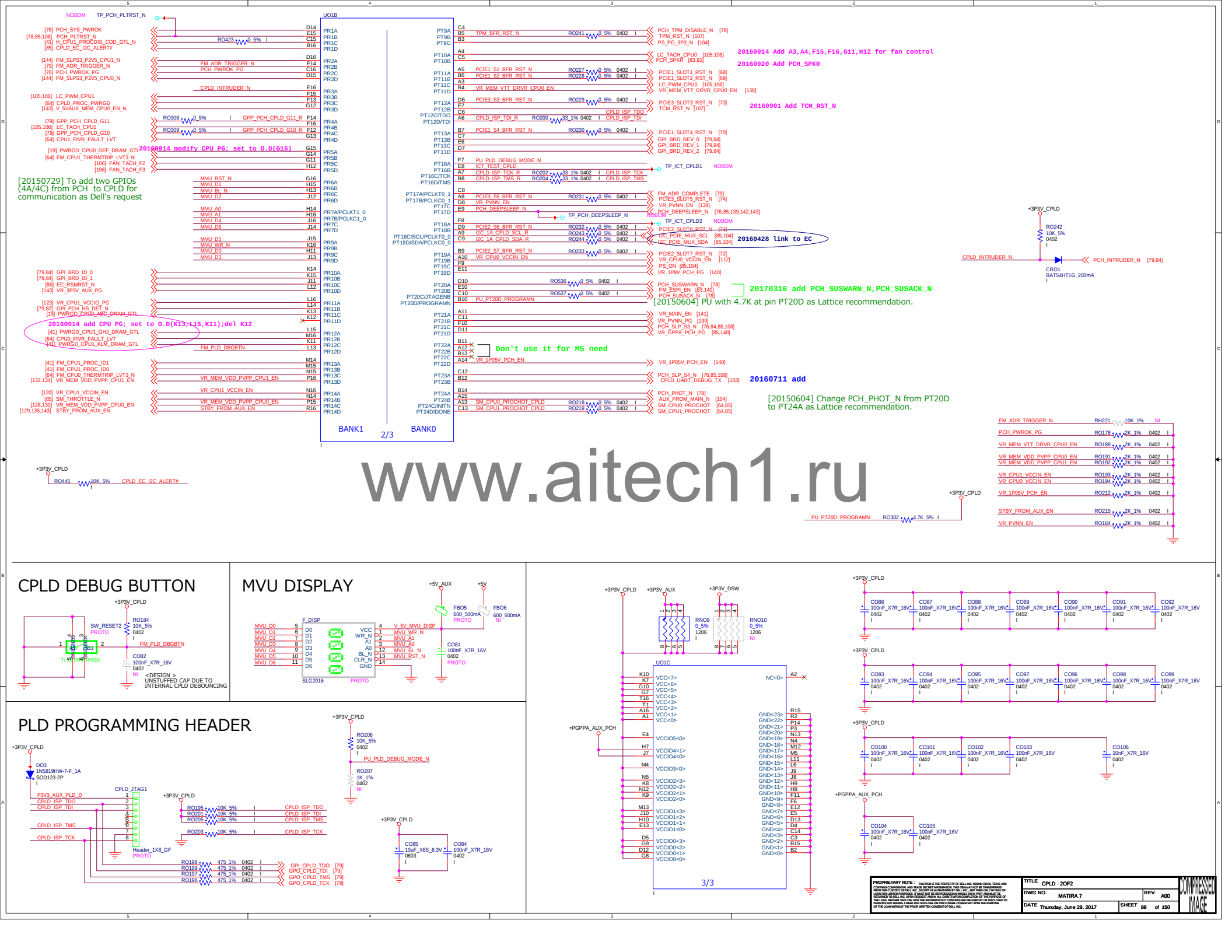
COMPRESSED IMAGE



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TITLE	CPLD - 2OF2
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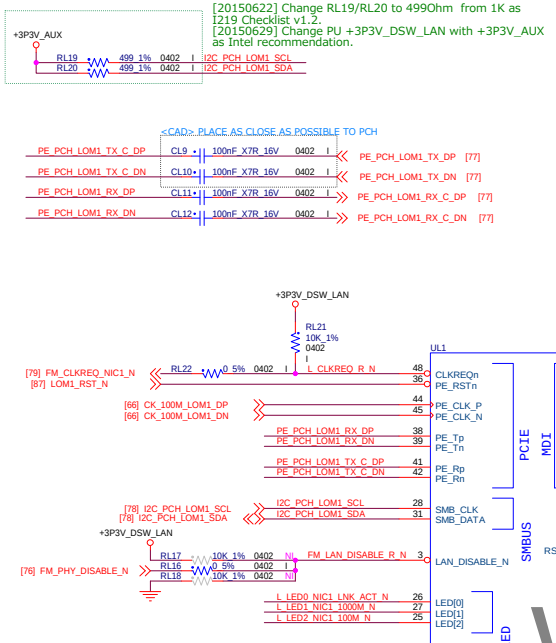
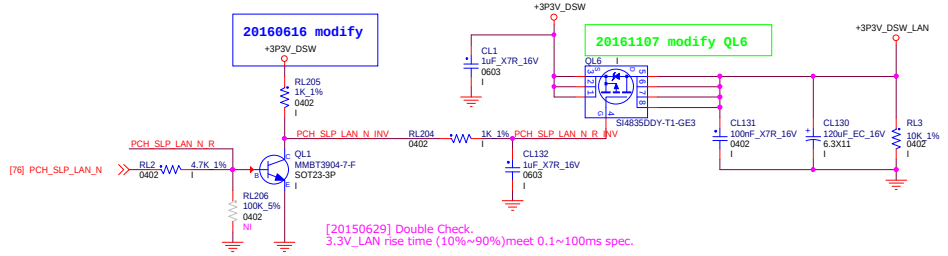
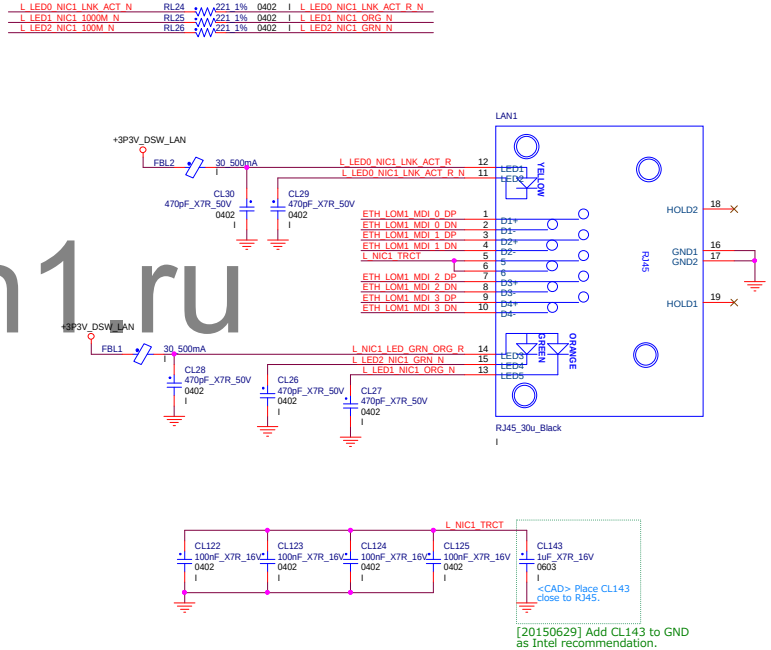
Jacksonville / I219 (PHY)



I219 LOM Power





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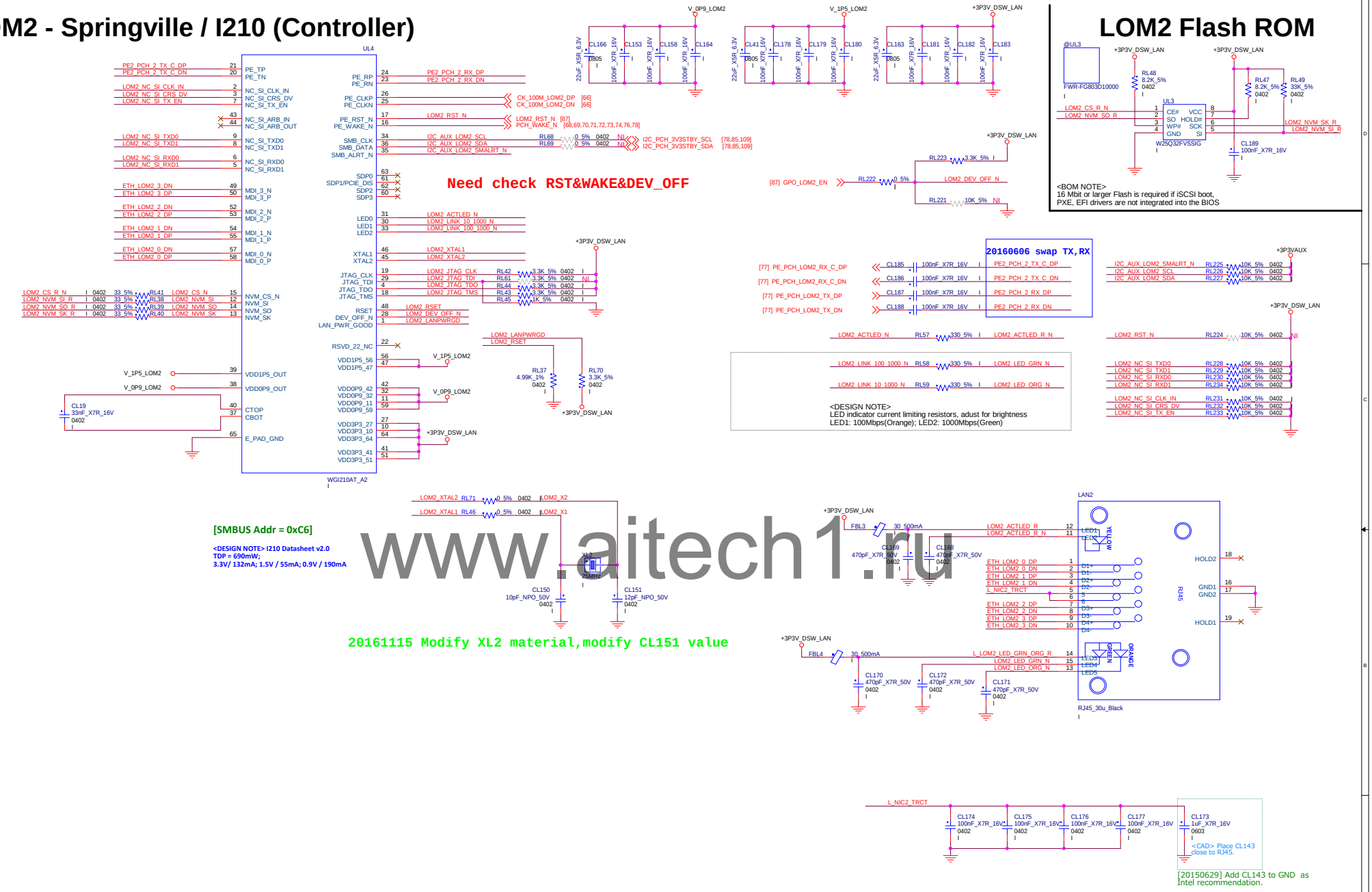
LOM2 - Springville / I210 (Controller)



LOM2 Flash ROM

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[20150629] Add CL143 to GND as Intel recommendation.

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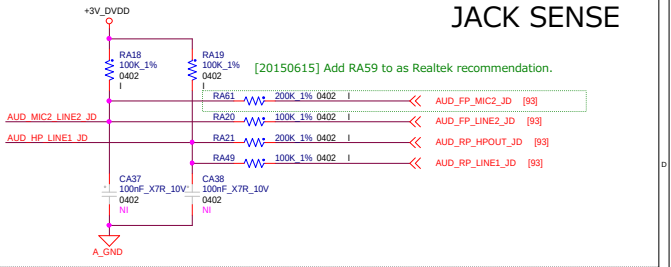
CUSTOMER ISSUE

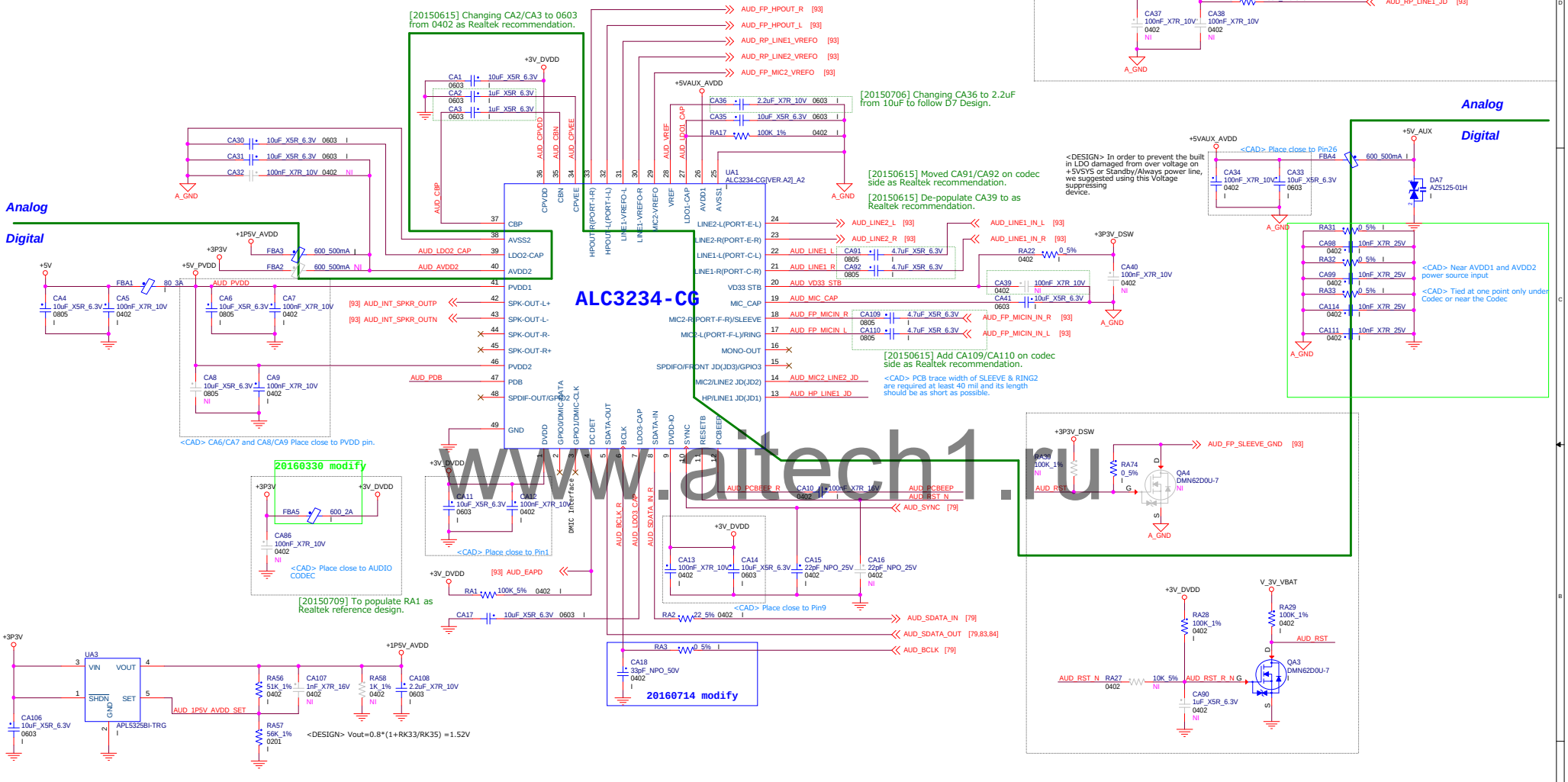
Audio Codec

JACK SENSE

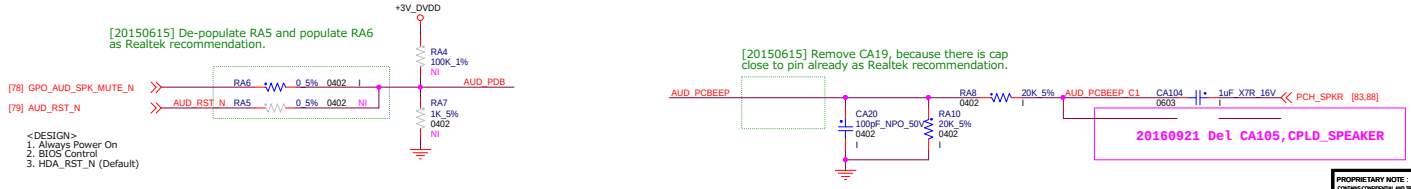


Analog

Digital



Amplifier Power Down Options



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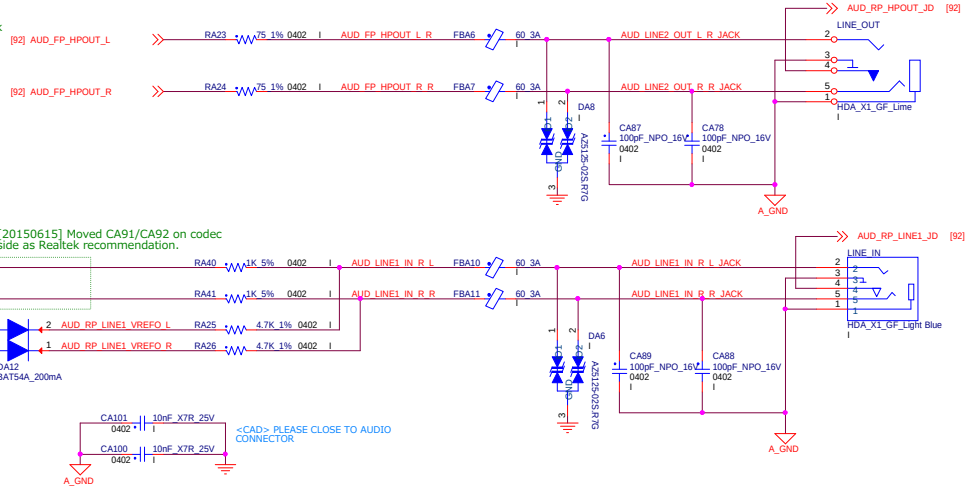
REAR PANEL

[20150709] Updated the schematic for Rear Panel as Realtek recommendation.

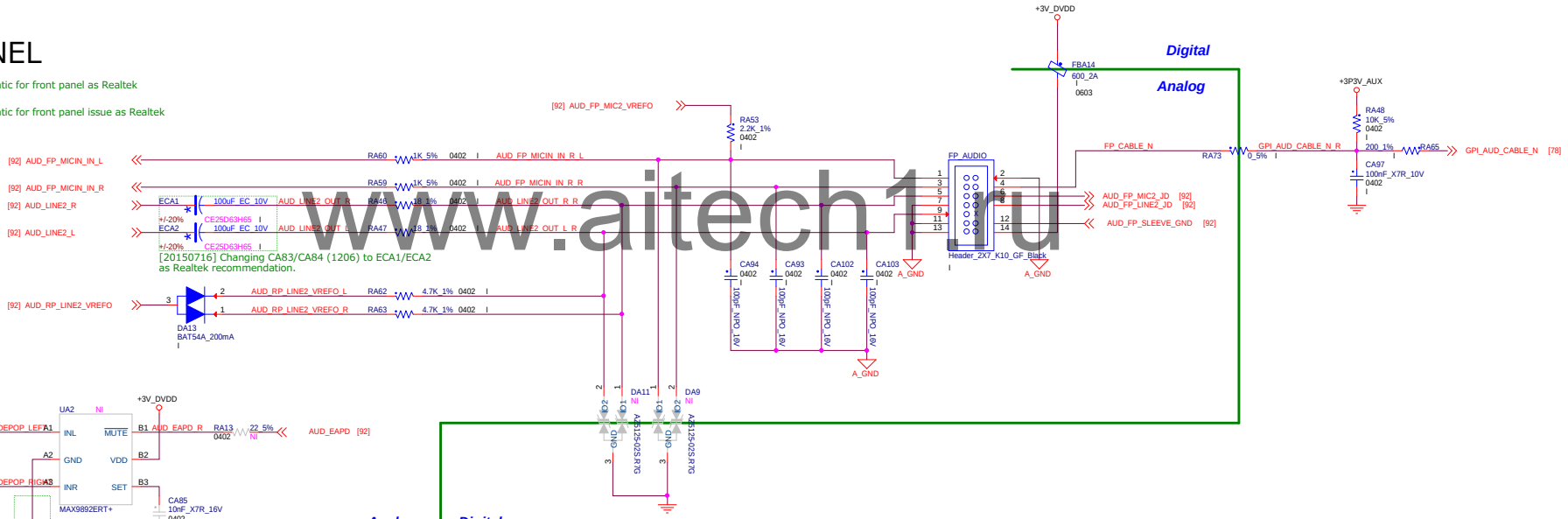


20161107 Del Add FP_AUDIO1 and peripheral component

FRONT PANEL

[20150615] Updated the schematic for front panel as Realtek recommendation.

[20150709] Updated the schematic for front panel issue as Realtek recommendation.



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ARD v0.25

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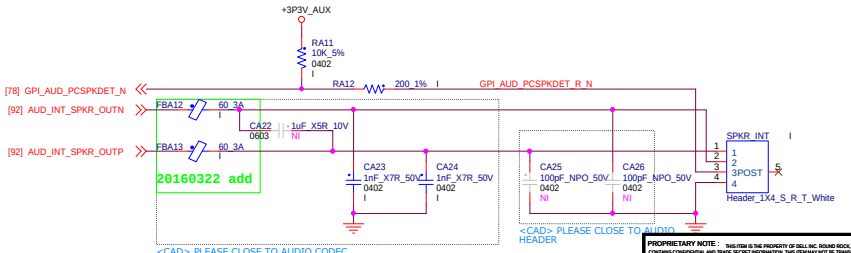
CHASSIS SPEAKER



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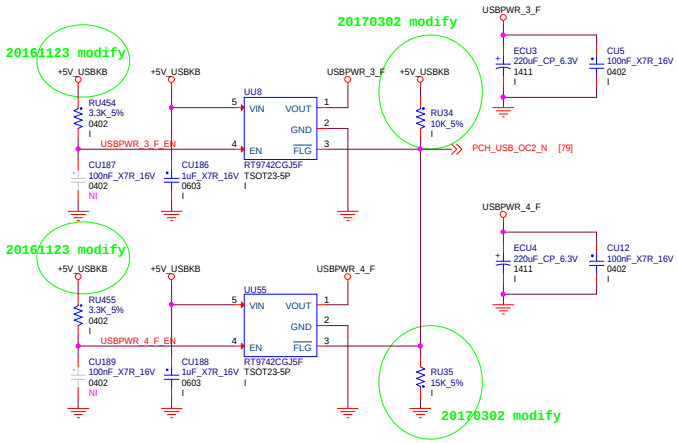
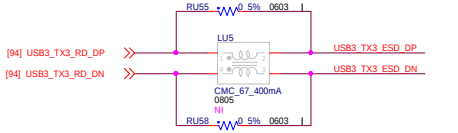
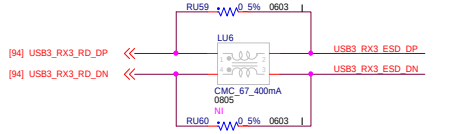
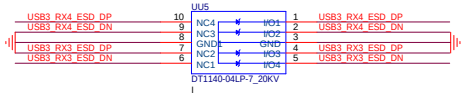
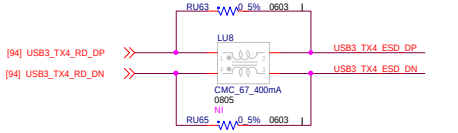
Rear USB3.0 Connector 1OF3

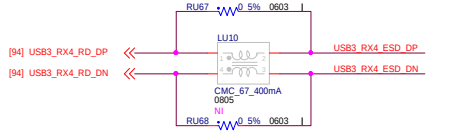


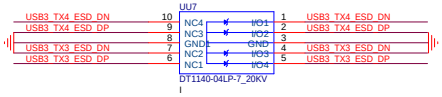


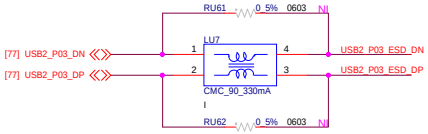


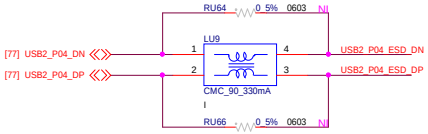


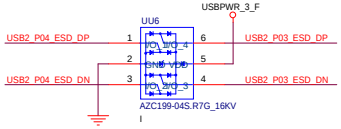




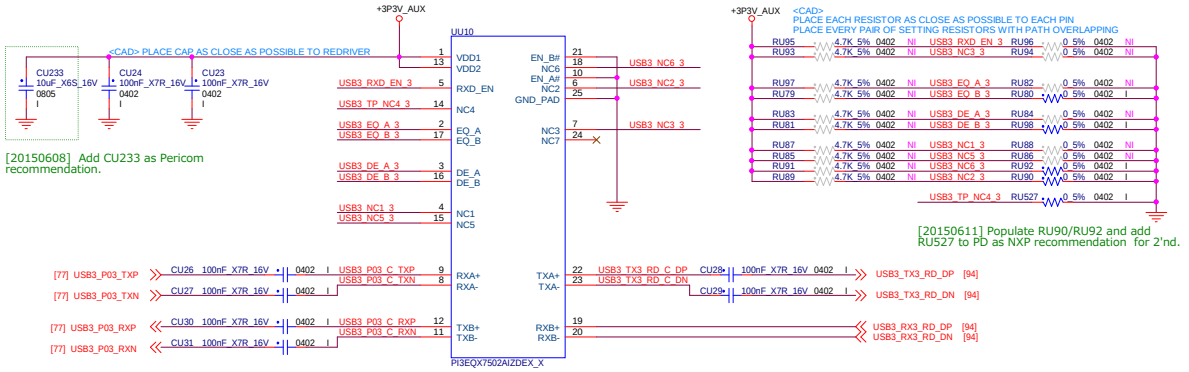


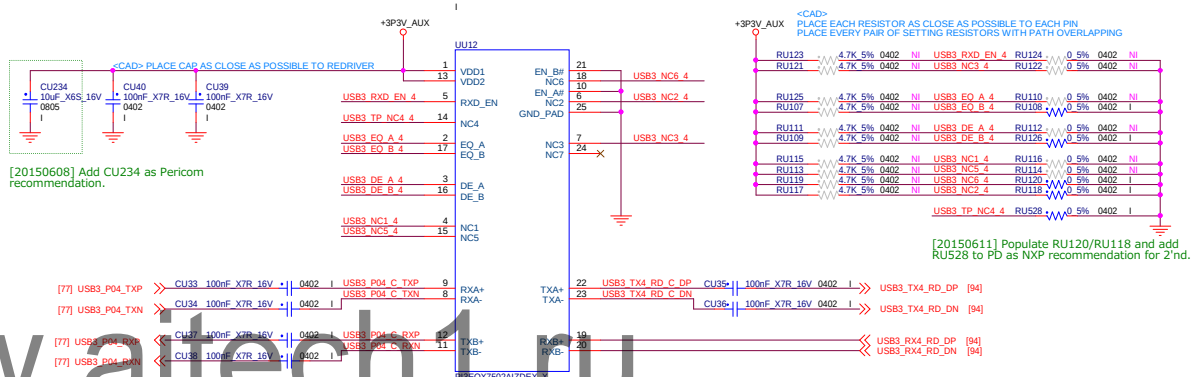


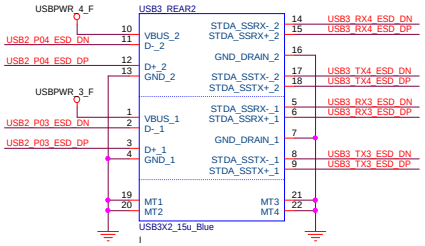




USB3.0 REDRIVER







Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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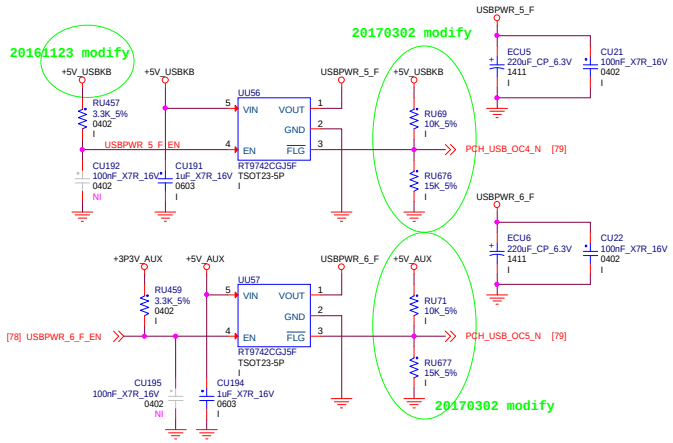
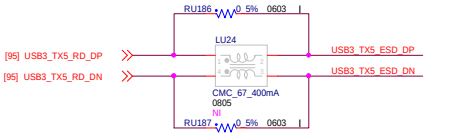
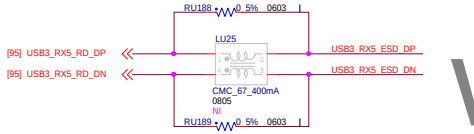
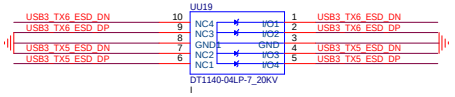
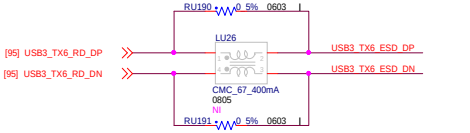
Rear USB3.0 Connector 2OF3

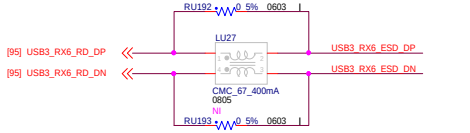


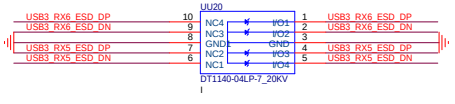


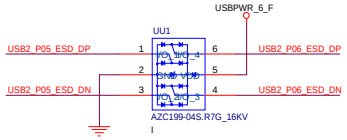


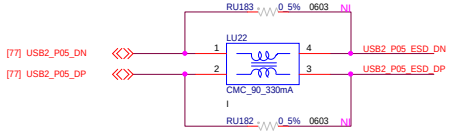


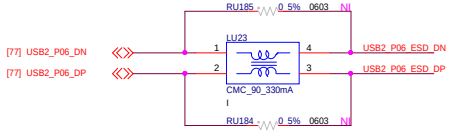


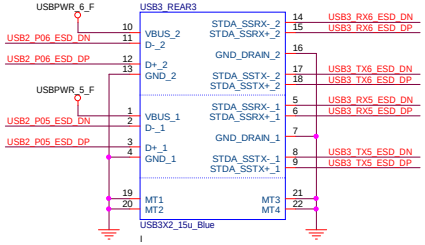




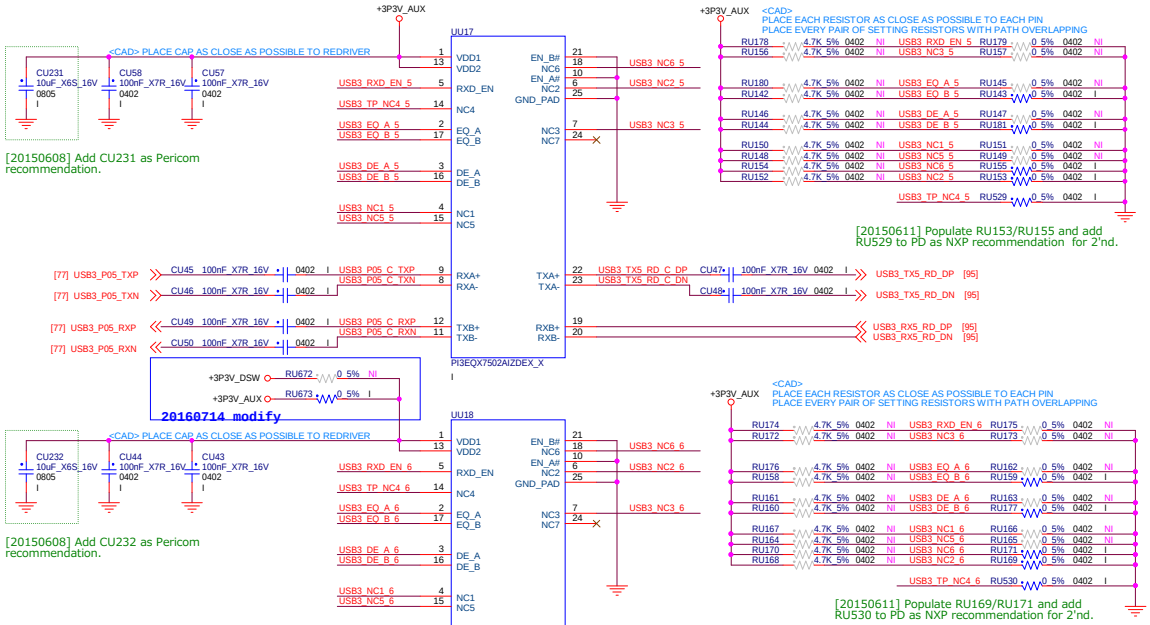








USB3.0 REDRIVER



Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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TITLE	USB 3.0 Connector - 2 OF 3
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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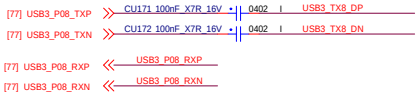
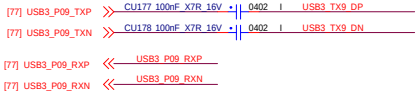
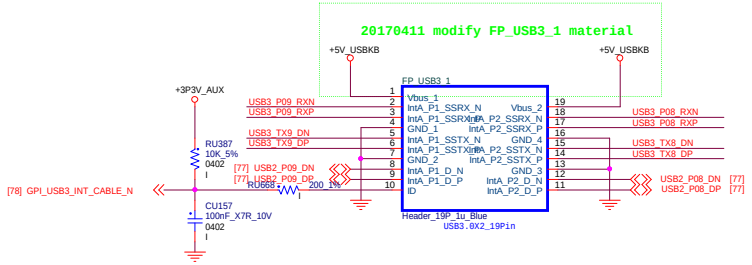
COMPUTER IMAGE

Front Panel USB3_1 for HUB and SD card

www.aitech1.ru







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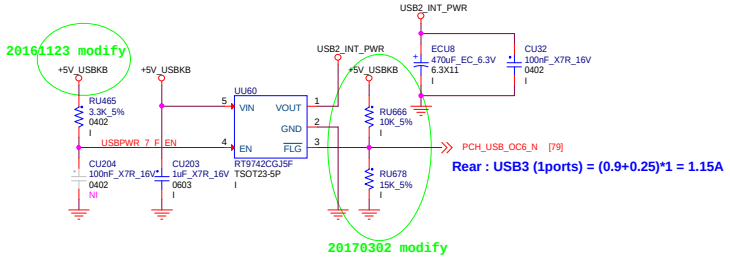
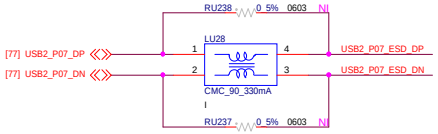
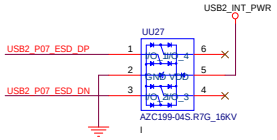
TITLE	Front Panel USB3_1		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	96 of 150

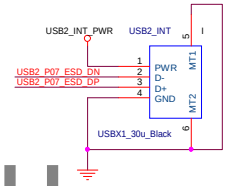
COMPRESSED IMAGE

INT USB2.0 Connector









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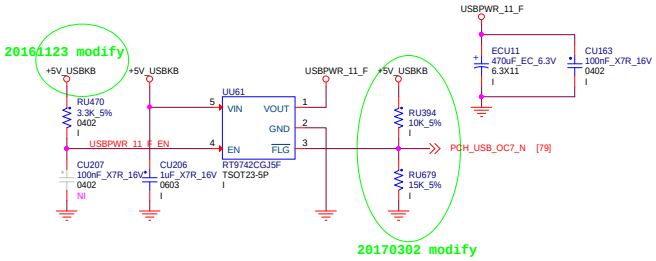
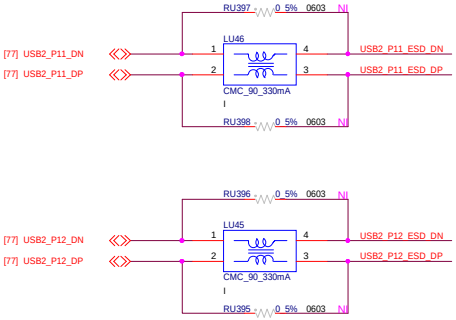
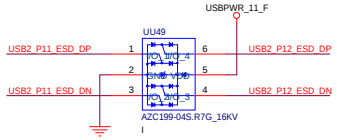
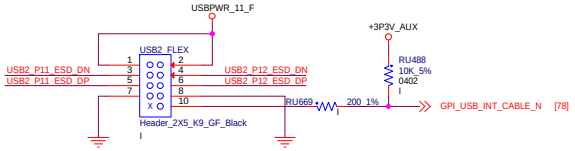
INT USB2.0 Card Reader Header









20170315 modify USB2_FLEX component

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TITLE	INT USB 2.0
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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COMPRESSED IMAGE

Front Panel USB3_2 for Type C

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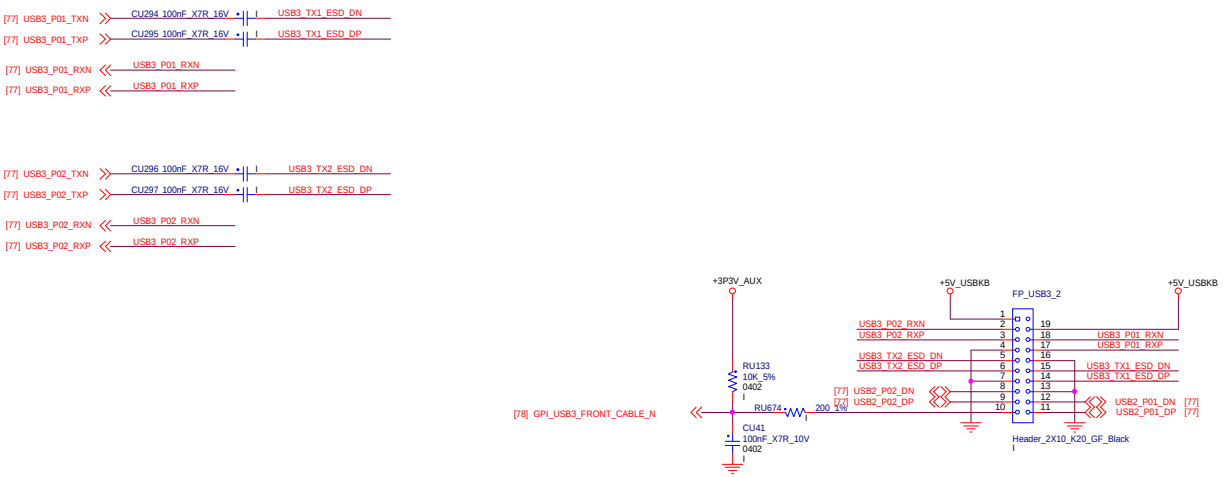

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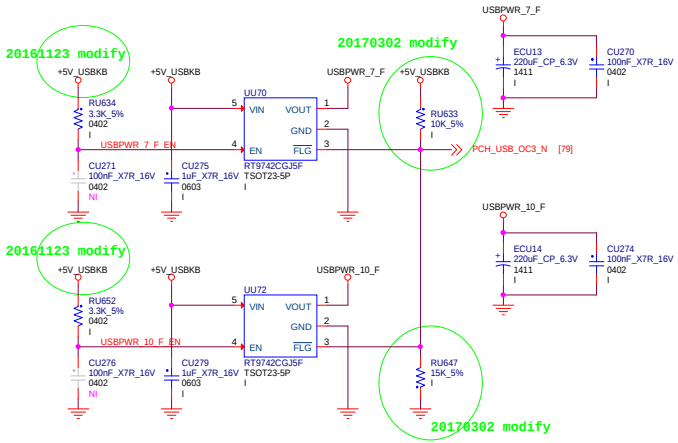
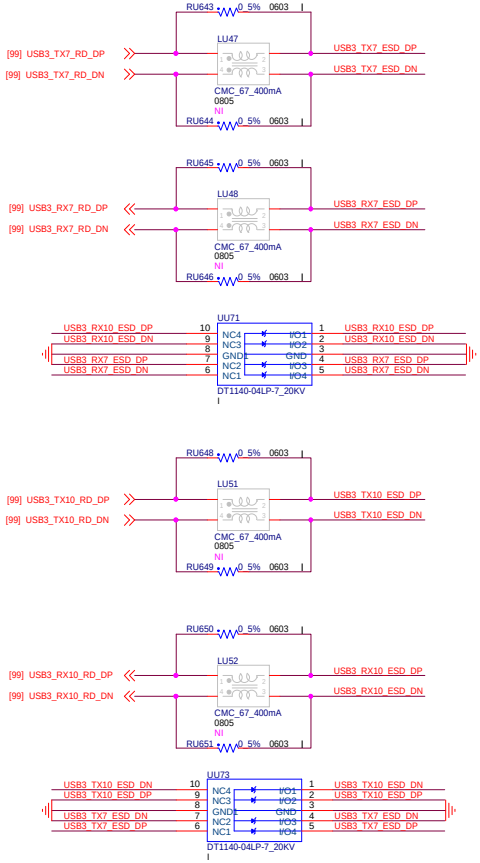
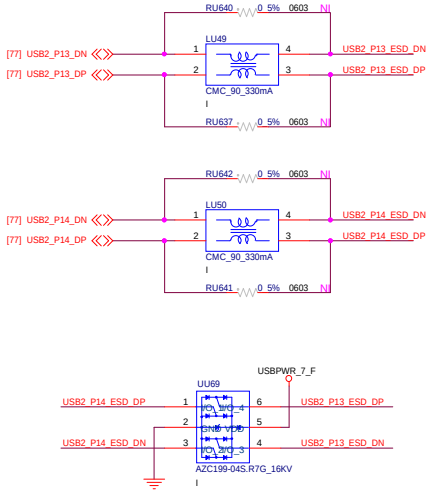
TITLE	Front Panel USB3_2		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	98 of 150

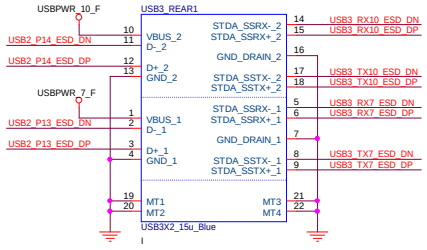
COMPRESSED IMAGE

Rear USB3.0 Connector 3OF3

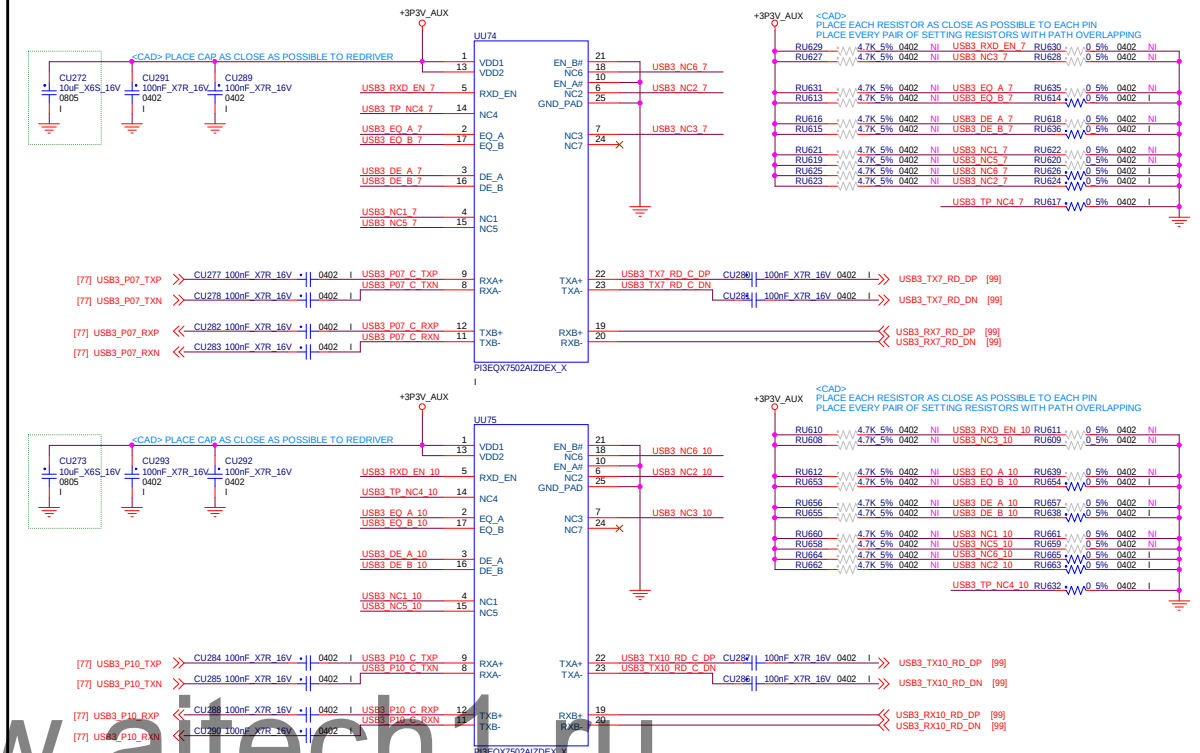








USB3.0 REDRIVER



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Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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TITLE	USB 3.0 Connector - 3 OF 3
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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COMPRESSED IMAGE

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TITLE	Blank	
DWG NO.	MATIRA 7	REV. A00
DATE	Thursday, June 29, 2017	SHEET 100 of 150

BLANK

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TITLE Blank		
DWG NO. MATIRA 7	REV. A00	
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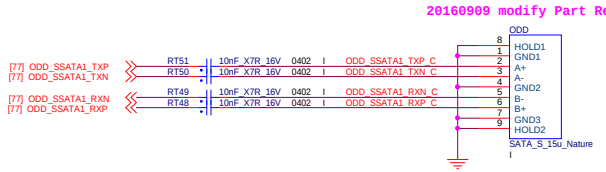
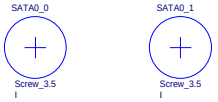
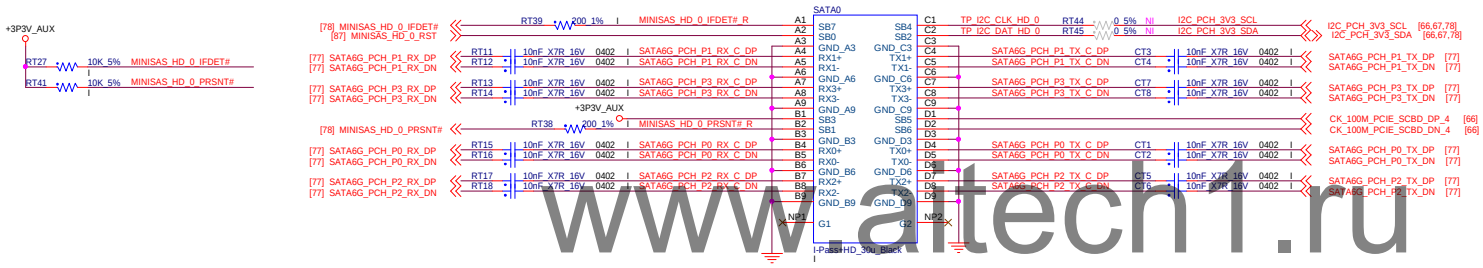
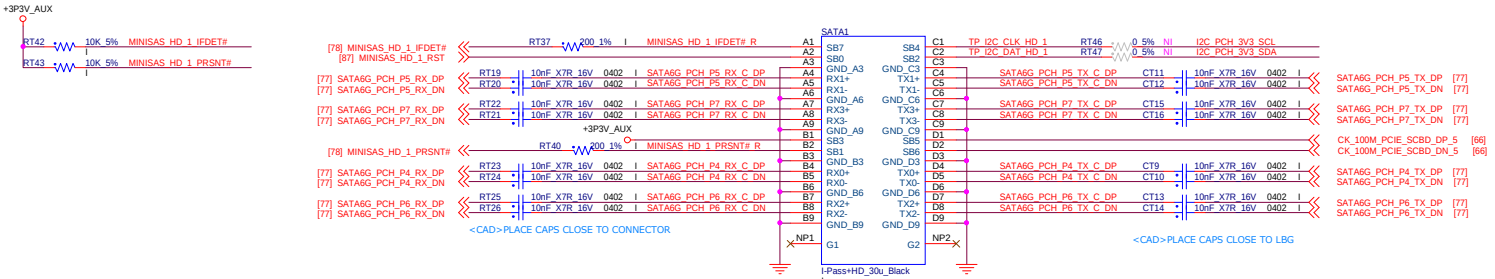
PCH PCIE Storage Connector

20160909 modify Part Reference

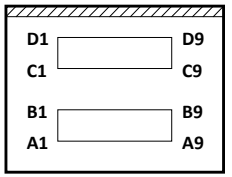








Mini SAS HD 4i receptacle connector



Footprint: minisas36sh124_avalon
(increased 0.3mm pin width on G1/G2/G3/G4)

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TITLE	SATA Connector
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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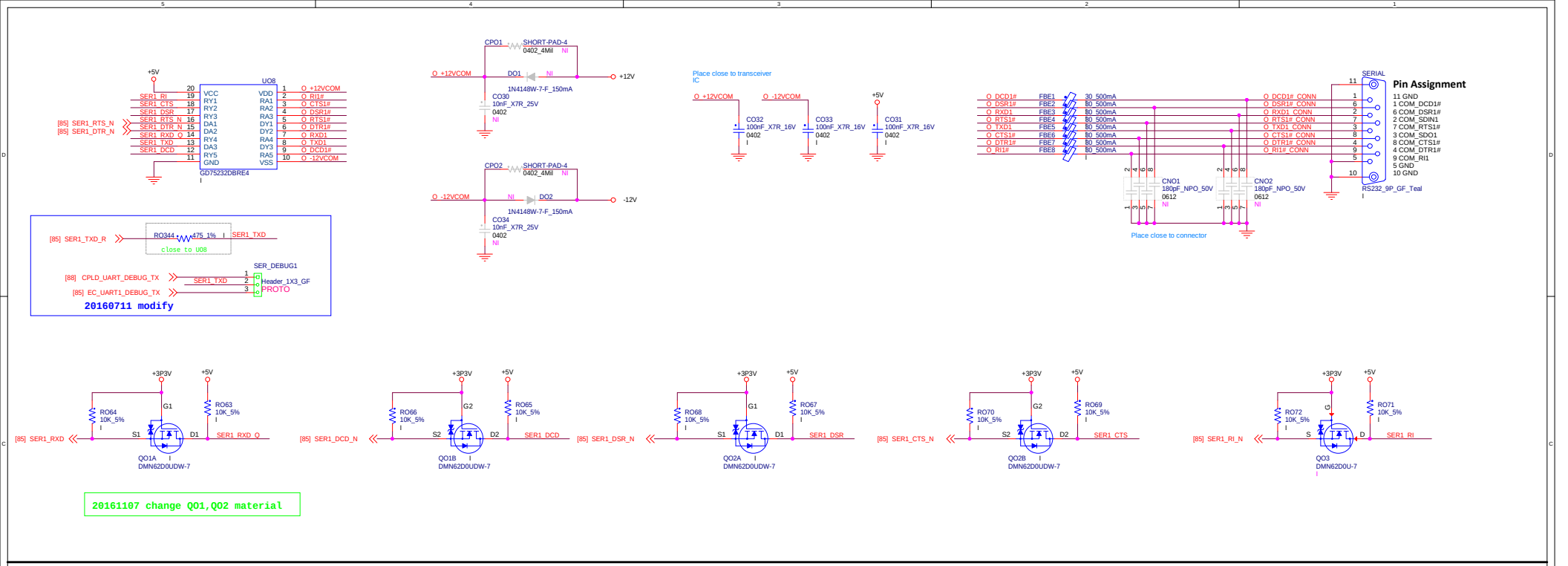
COMPRESSED IMAGE



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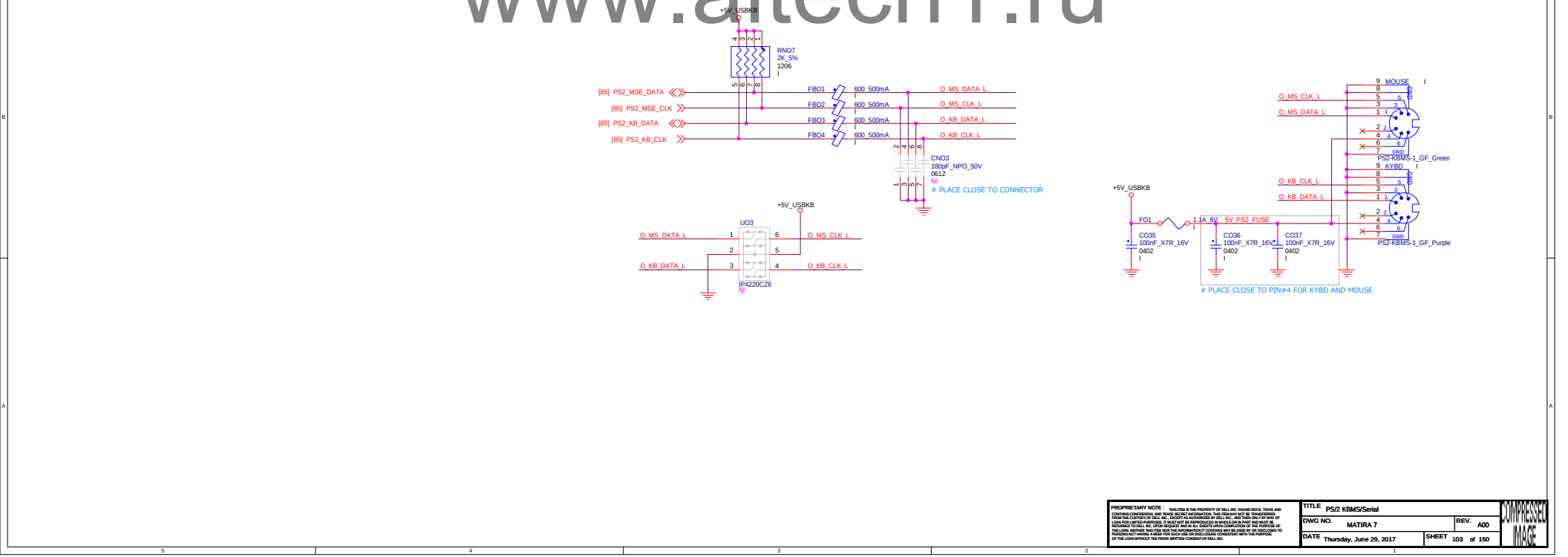

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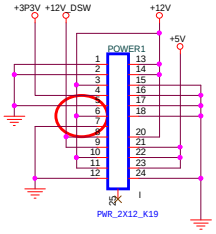
TITLE	PS/2 KBMS/Serial
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	103 of 150

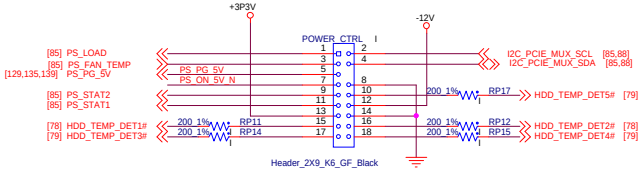
COMPRESSED IMAGE

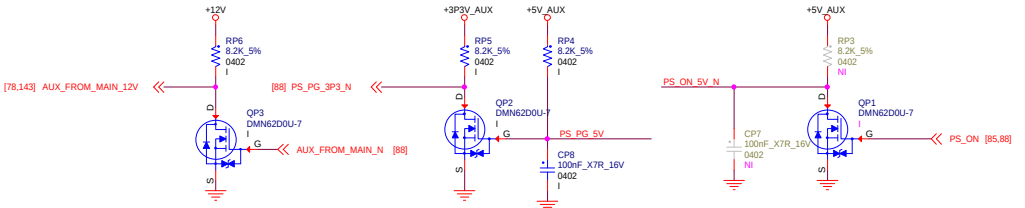
POWER1 Connector

Modify 11/05

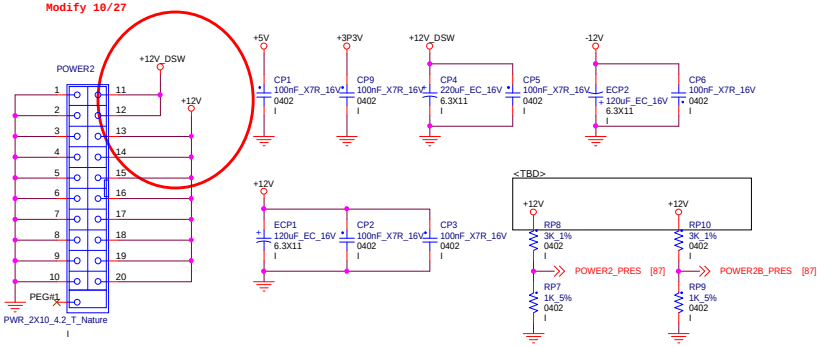


20160909 modify part reference





Modify 10/27



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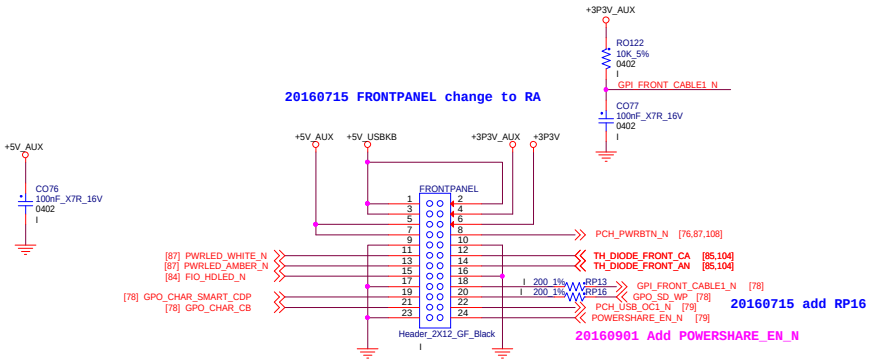
FRONTPANEL

20160426 del OCU_FRONT and peripheral component

20160715 FRONTPANEL change to RA



20160715 add RP16

20160901 Add POWERSHARE_EN_N

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TITLE	Power Conn/Front Panel
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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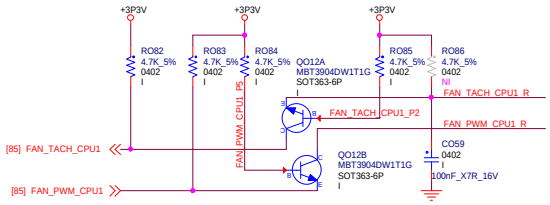
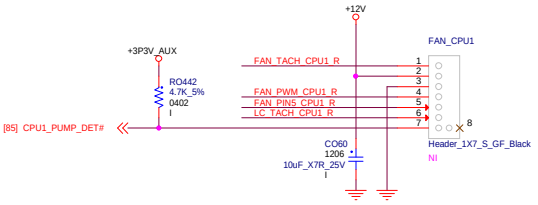
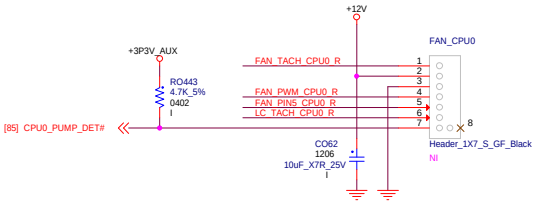
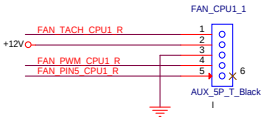
COMPUTER IMAGE

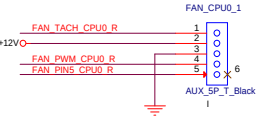
For only 1 CPU Fan

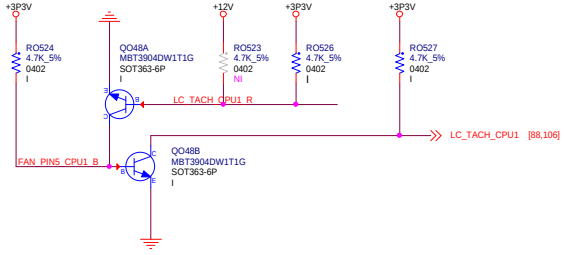




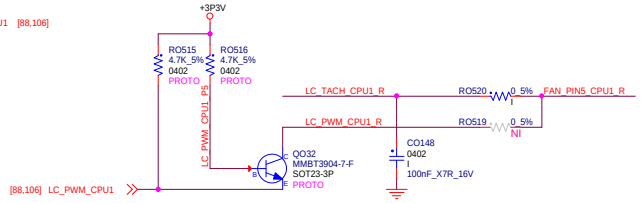




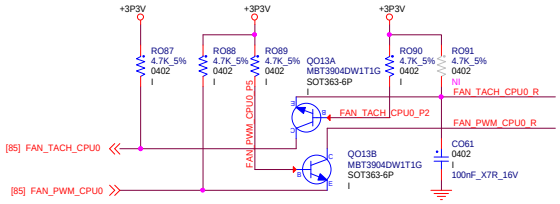




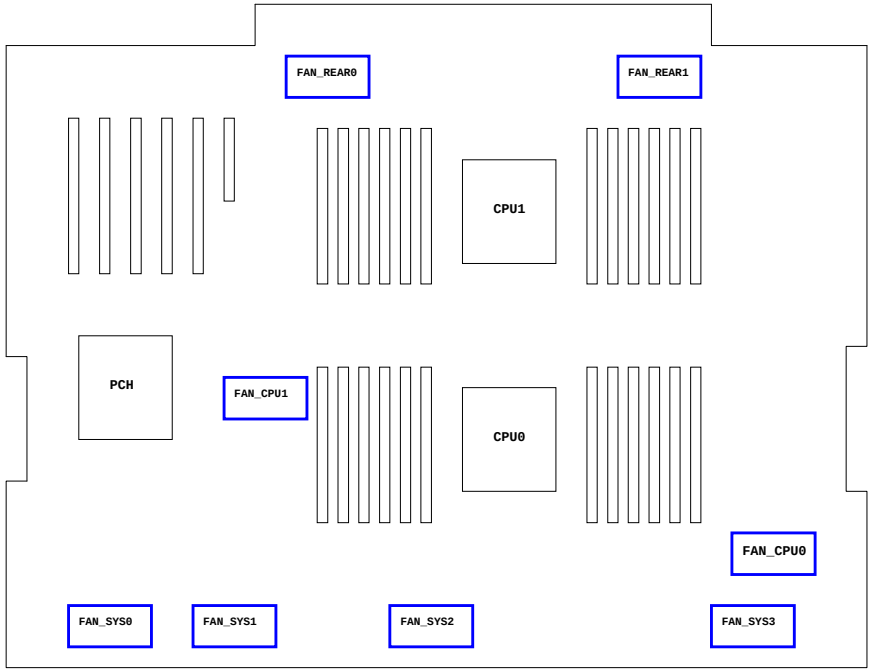
FAN 5Pin	RO520 Install RO519 Non-install (Default)	Compatible with Avalon3,PUMP can be monitored and indirectly detected,but not controlled
FAN 7Pin	RO520 Non-install RO519 Install RO526 Install	Not compatible with Avalon3,PUMP can be monitored,detected and controlled

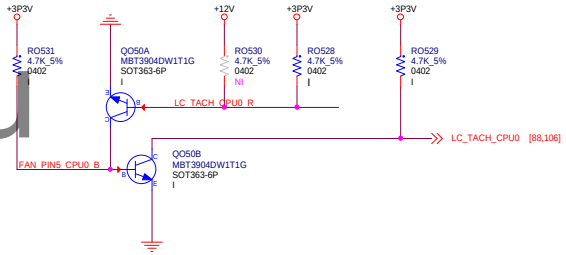


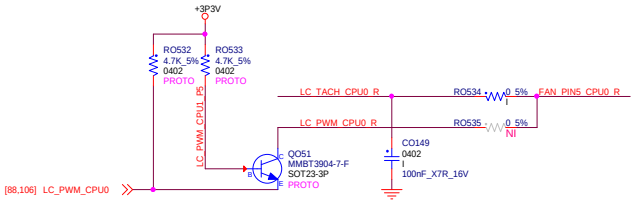
20161116 Add



www.aitech1.ru







20161116 Add

FAN 5Pin	RO534 Install RO535 Non-install (Default)	Compatible with Avalon3,PUMP can be monitored and indirectly detected,but not controlled
FAN 7Pin	RO534 Non-install RO535 Install RO528 Install	Not compatible with Avalon3,PUMP can be monitored,detected and controlled

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TITLE	Fan Conector_1
DWG NO.	MATIRA 7
REV.	A00
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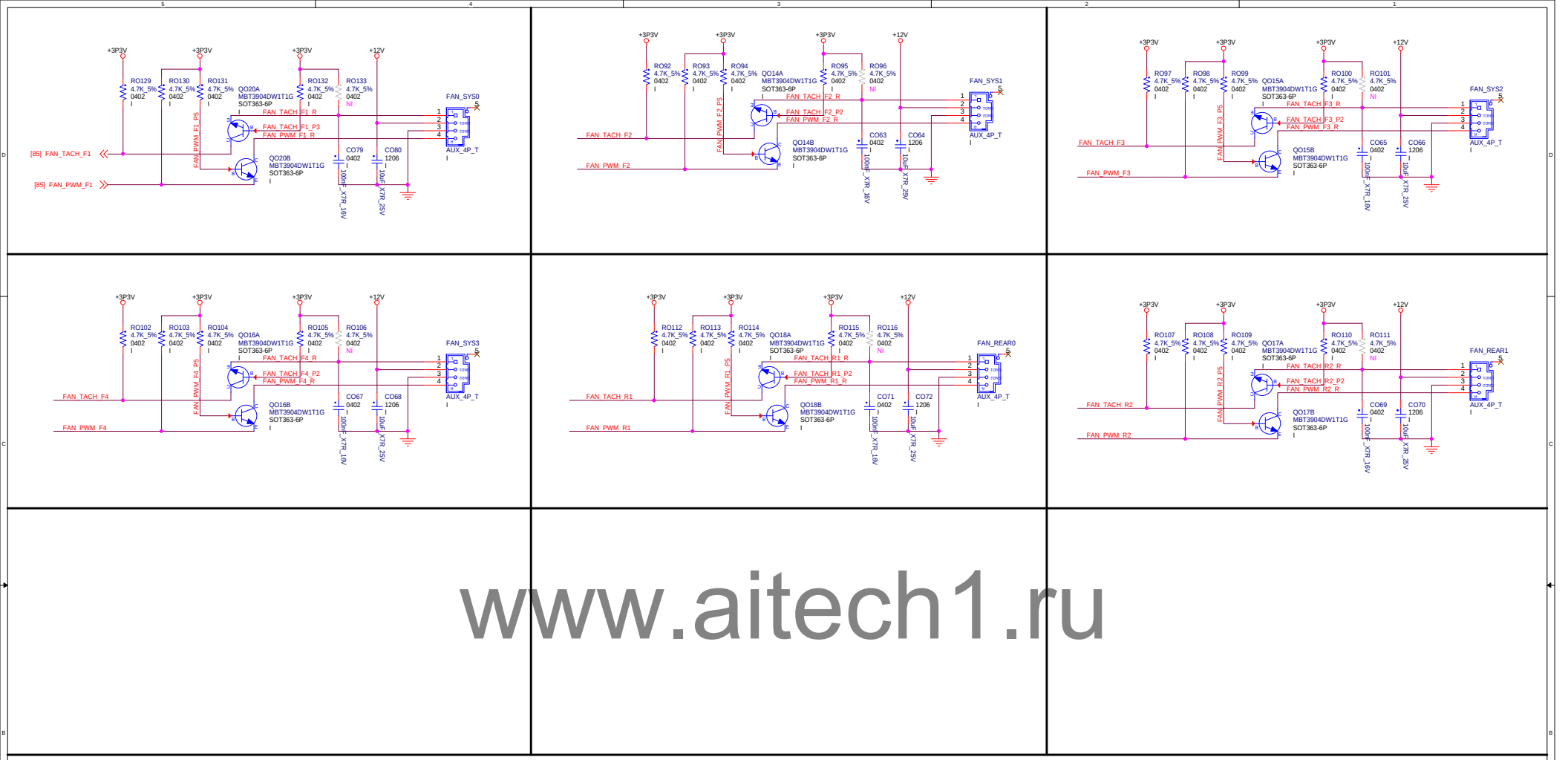
COMPOSITE IMAGE



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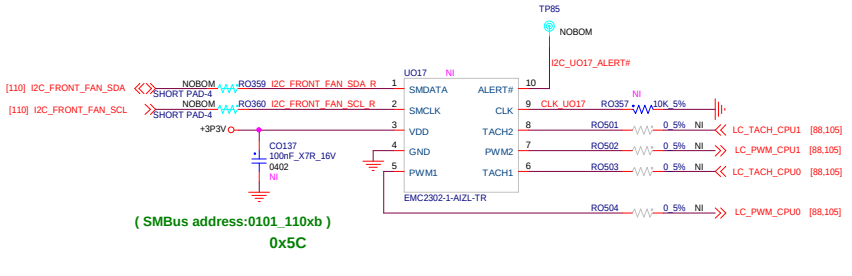

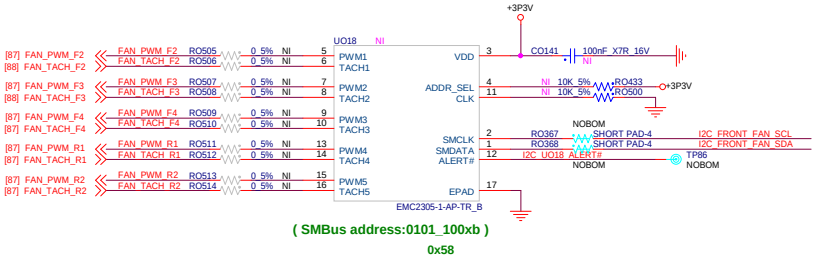

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TITLE	Fan Conector_2
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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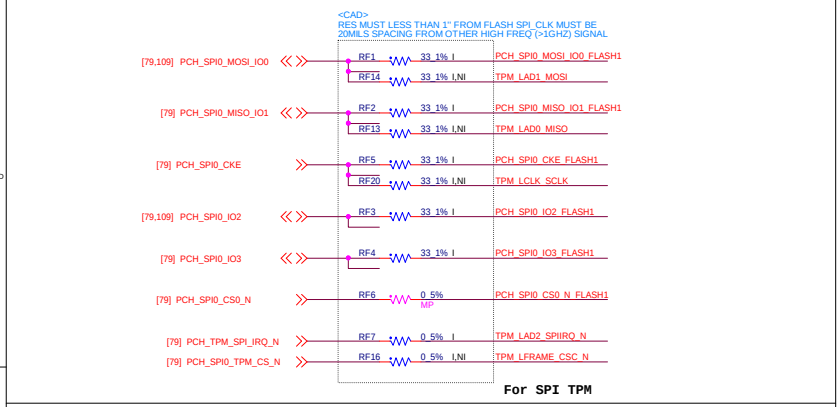
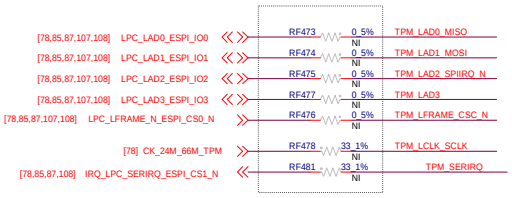
COMPRESSED IMAGE

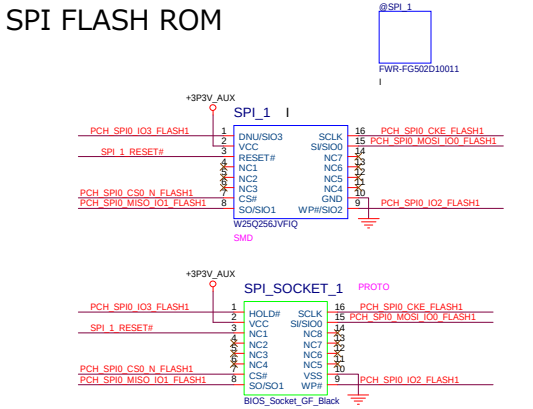


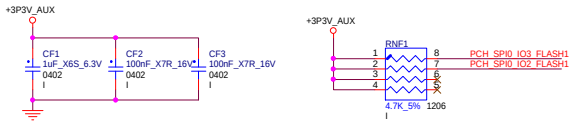
For SPI TPM



For LPC TPM

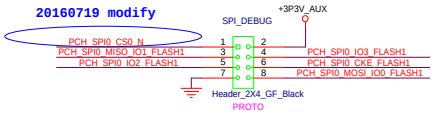
SPI FLASH ROM



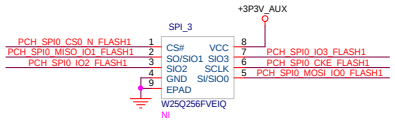


SPI ROM DEBUG HEADER/JUMPER

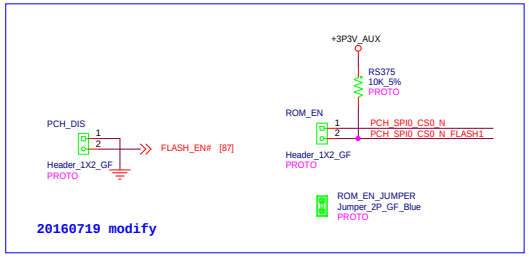
20160719 modify



20160516 modify SPI_DEBUG pin definite



20160721 Update SPI_3 library



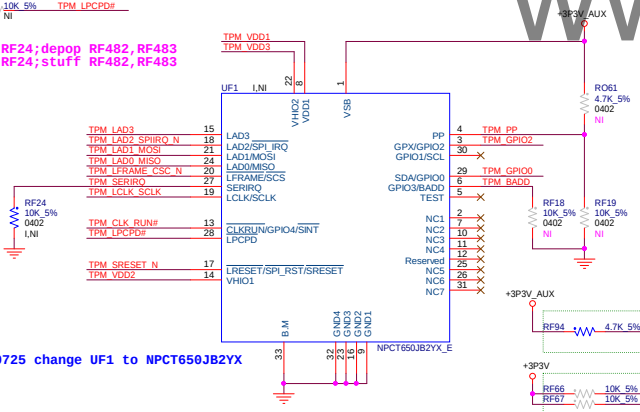
20160719 modify

SPI ROM Truth Table

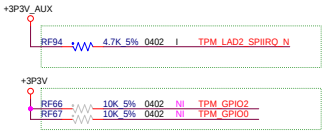
PCH_DIS	ROM_EN	Function
Open	Install	Onboard ROM boot
Open	Open	SPI Emulator Boot
Install	Open	No boot
Install	Install	DediProg update Onboard ROM

TPM 1.2

SPI:stuff RF24;depop RF482,RF483
LPC:depop RF24;stuff RF482,RF483



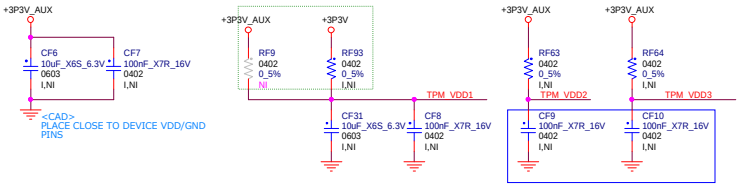
20160725 change UF1 to NPCT650JB2YX



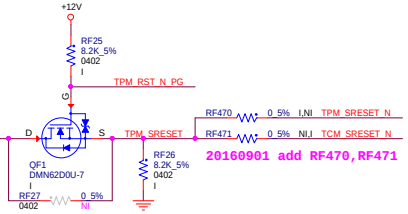
[20150611] Change the PU resistance to close Pin18 as Nuvoton recommendation.

[20150615] De-popolate the RF66 as Nuvoton recommendation.

[20150611] Reserve PU to +3P3V for TPM_VDD1 as Nuvoton recommendation.
[20150615] Populate RF93 and de-populate RF9 and add CF31 as Nuvoton recommendation.

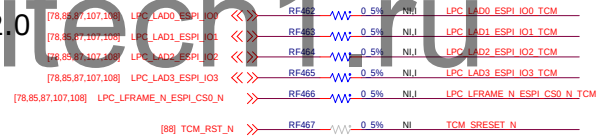


20160702 Nuvoton Adel Cheng recommend to 0.1uF from 1uF



20160901 add RF470,RF471

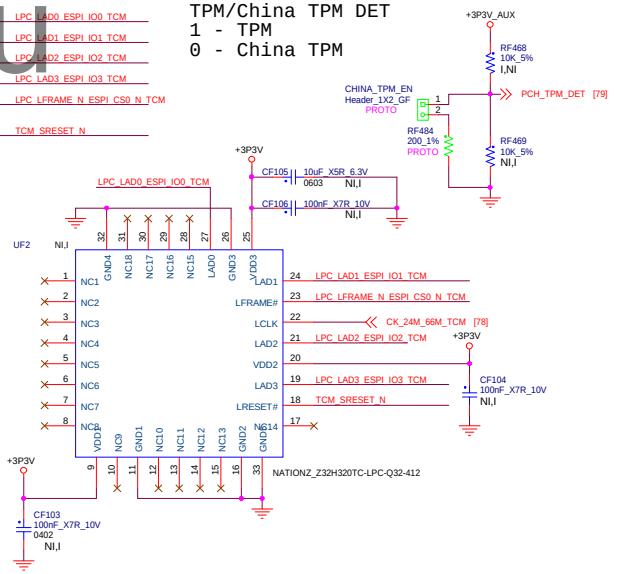
China TPM2.0



20160901 Add China TPM 2.0

TPM/China TPM DET

1 - TPM
0 - China TPM



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TITLE	TPM/China TPM/SPI
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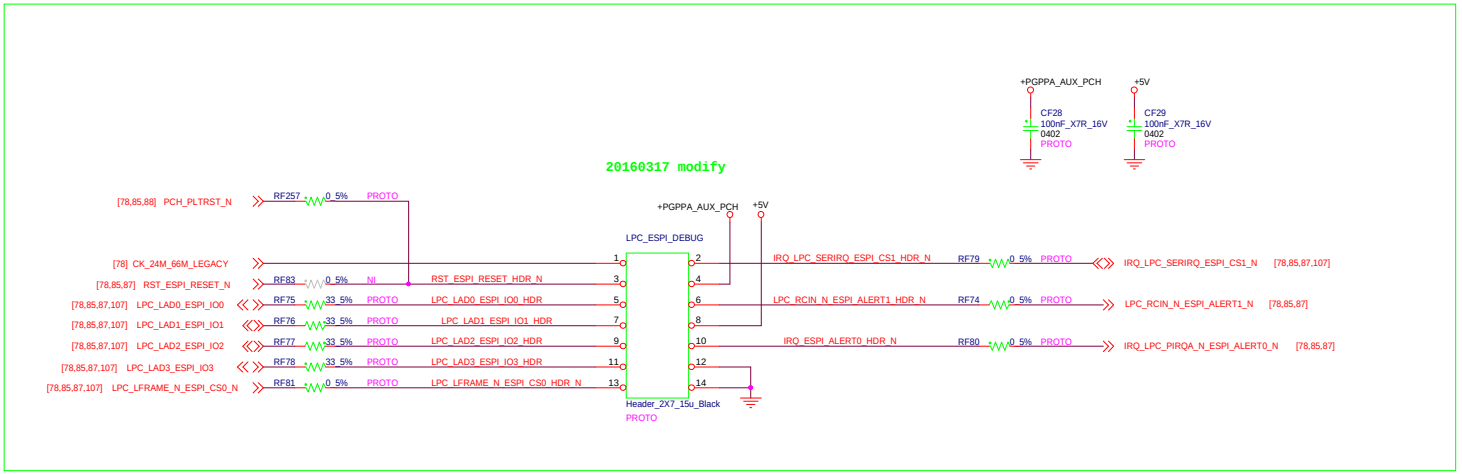
COMPRESSED IMAGE

LPC/ESPI DEBUG HEADER



Licence Label

Note:
AMI uEFI

20170315 modify
20170327 Remove BIOS_LABEL
20170405 Add BIOS_LABEL for BPM cost price

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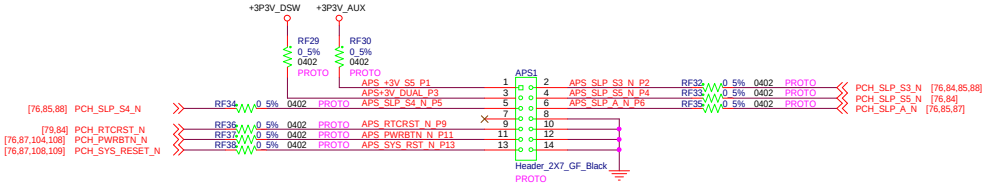
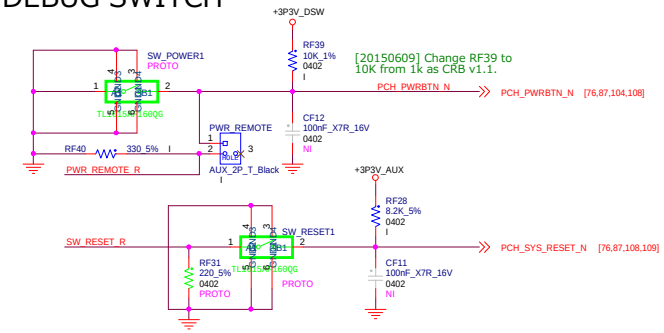
APS HEADER

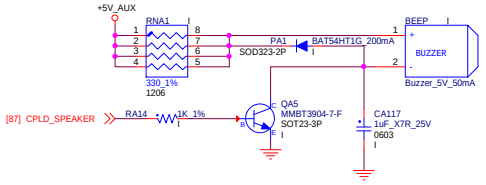


DEBUG SWITCH



BUZZER

20160920 Modify BUZZER schematic



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TITLE	Debug/Label/Misc
DWG NO.	MATIRA 7
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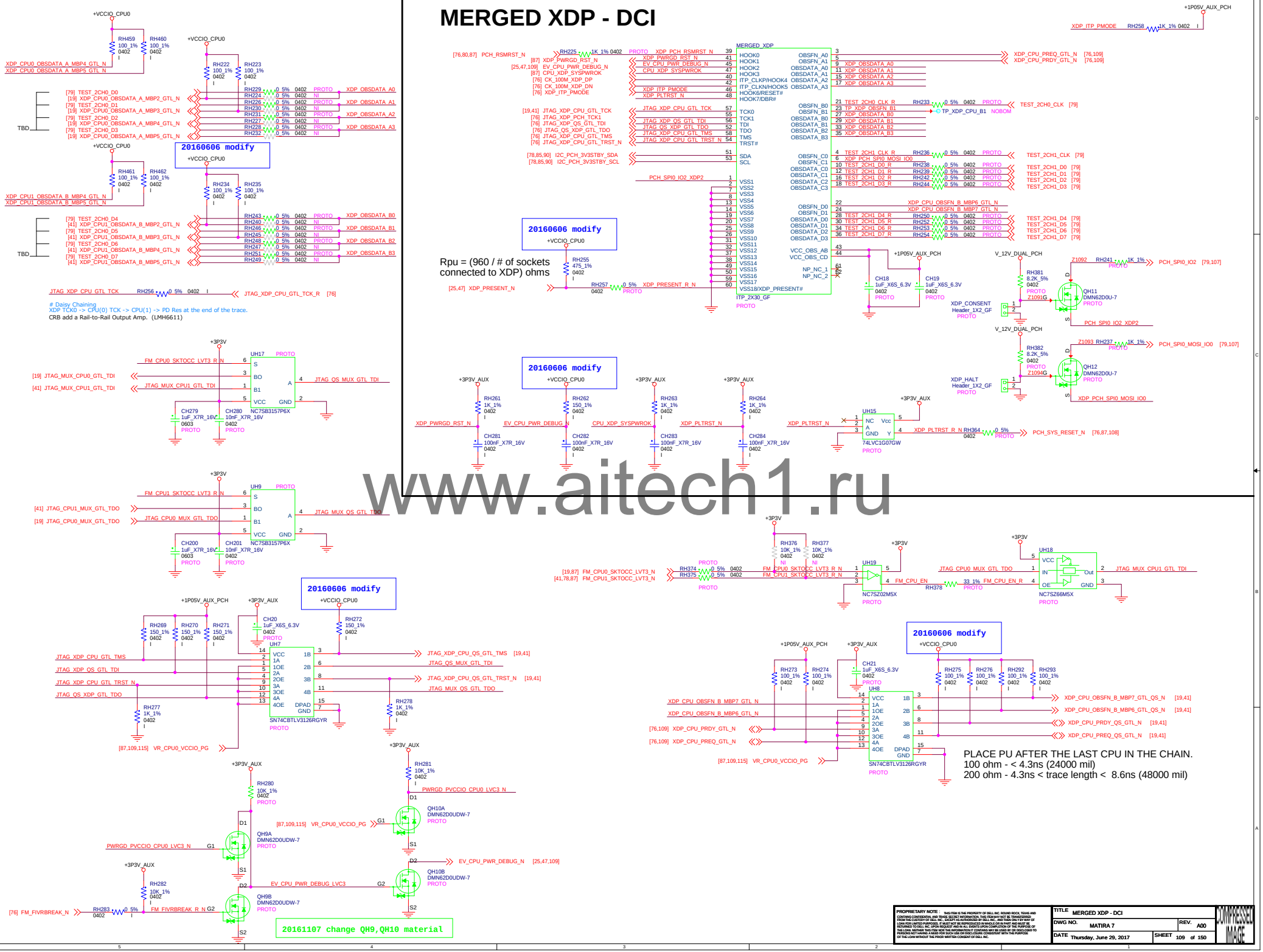
COMPUCESE IMAGE

MERGED XDP - DCI



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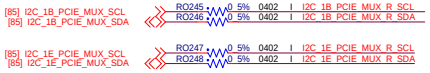
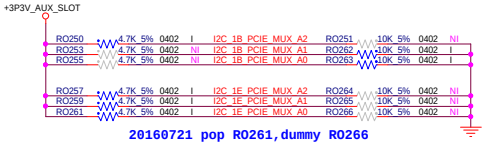
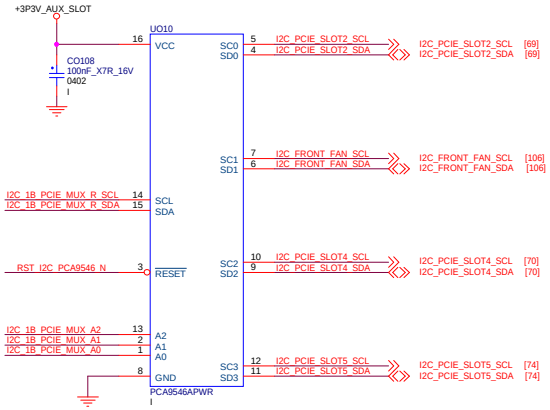
SMBUS MUX



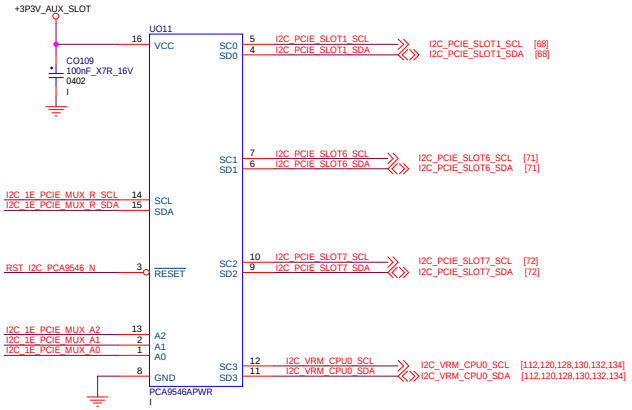


20160721 pop RO261,dummy RO266



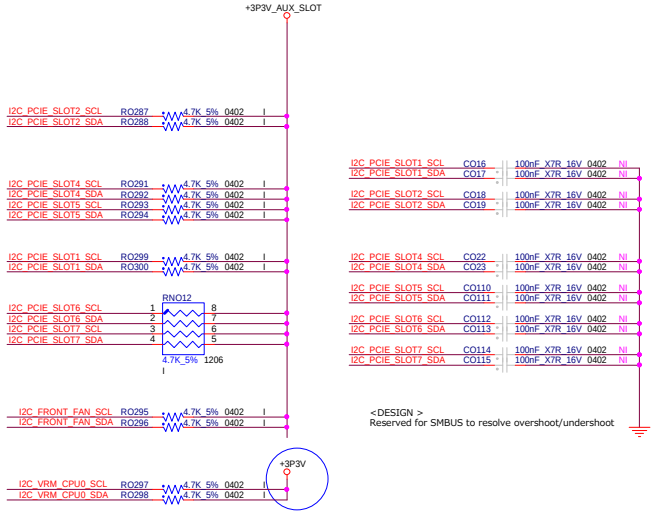
(SMBus address:1110_100xb)

0xE8

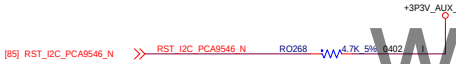


(SMBus address:1110_111xb)

0xEE



20160722 modify to +3P3V



20160908 Add RST_I2C_PCA9546_N

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COMPRESSED IMAGE

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TITLE	SMBUS MUX		
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COMPRESSED IMAGE

Insertion Loss Measurement

L1/85ohm/15% — L1_85_MS — L1_85_MS

L1/100ohm/10% — L1_100_MS — L1_100_MS

L3/85ohm/10% — L3_85_SL — L3_85_SL

L3/100ohm/10% — L3_100_SL — L3_100_SL

L6/85ohm/10% — L6_85_SL — L6_85_SL

L6/100ohm/10% — L6_100_SL — L6_100_SL

L8/85ohm/15% — L8_85_MS — L8_85_MS

L8/100ohm/10% — L8_100_MS — L8_100_MS

L1_85_MS_THROUGH — S_85_MS_THROUGH

L1_100_MS_THROUGH — S_100_MS_THROUGH

Impedance Control Test Coupon

L1/80ohm/10% — Z_L1_80_MS Header_1X2_GF NI — Z_L1_80_MS_DP / Z_L1_80_MS_DN — Z_L1_80_MS_END Header_1X2_GF NI

L1/95ohm/15% — Z_L1_95_MS Header_1X2_GF NI — Z_L1_95_MS_DP / Z_L1_95_MS_DN — Z_L1_95_MS_END Header_1X2_GF NI

L8/80ohm/10% — Z_L8_80_MS Header_1X2_GF NI — Z_L8_80_MS_DP / Z_L8_80_MS_DN — Z_L8_80_MS_END Header_1X2_GF NI

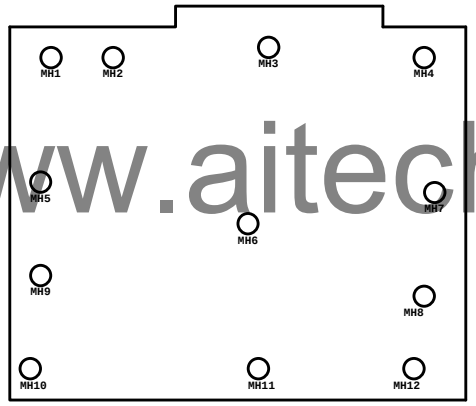
[20150728] To replace ZSE3PINS2R and MP_TP_1X3_35P with H2M-1 as Layout requirement.

MTG Holes

FD1 FMARK FD40 NOBOM
FD2 FMARK FD40 NOBOM
FD3 FMARK FD40 NOBOM
FD4 FMARK FD40 NOBOM
FD5 FMARK FD40 NOBOM
FD6 FMARK FD40 NOBOM
FD7 FMARK FD40 NOBOM
FD8 FMARK FD40 NOBOM

MOUNTING HOLES

MH1 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH2 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH3 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH4 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH5 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH6 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH7 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH8 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH9 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH10 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH11 NOBOM Mounting Hole — MH40X80_10_DELL_WS
MH12 NOBOM Mounting Hole — MH40X80_10_DELL_WS



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PCB — BTI_08EA25C48L I

PPID — Type_T_PPID_Label I

MH13 I Mounting Hole — MH_47_197_B77_M1_PTH
MH14 I Mounting Hole — MH_47_197_B77_M1_PTH
MH15 I Mounting Hole — MH_47_197_B77_M1_PTH
MH16 I Mounting Hole — MH_47_197_B77_M1_PTH
MH17 I Mounting Hole — MH_47_197_B77_M1_PTH

MH18 NOBOM Mounting Hole — NP126
MH19 NOBOM Mounting Hole — NP126
MH20 NOBOM Mounting Hole — NP126
MH21 NOBOM Mounting Hole — NP126
MH22 NOBOM Mounting Hole — NP126

MH23 NOBOM Mounting Hole — NP87
MH24 NOBOM Mounting Hole — NP87
MH25 NOBOM Mounting Hole — NP126
MH26 NOBOM Mounting Hole — NP114

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TITLE OTHER
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DATE Thursday, June 29, 2017
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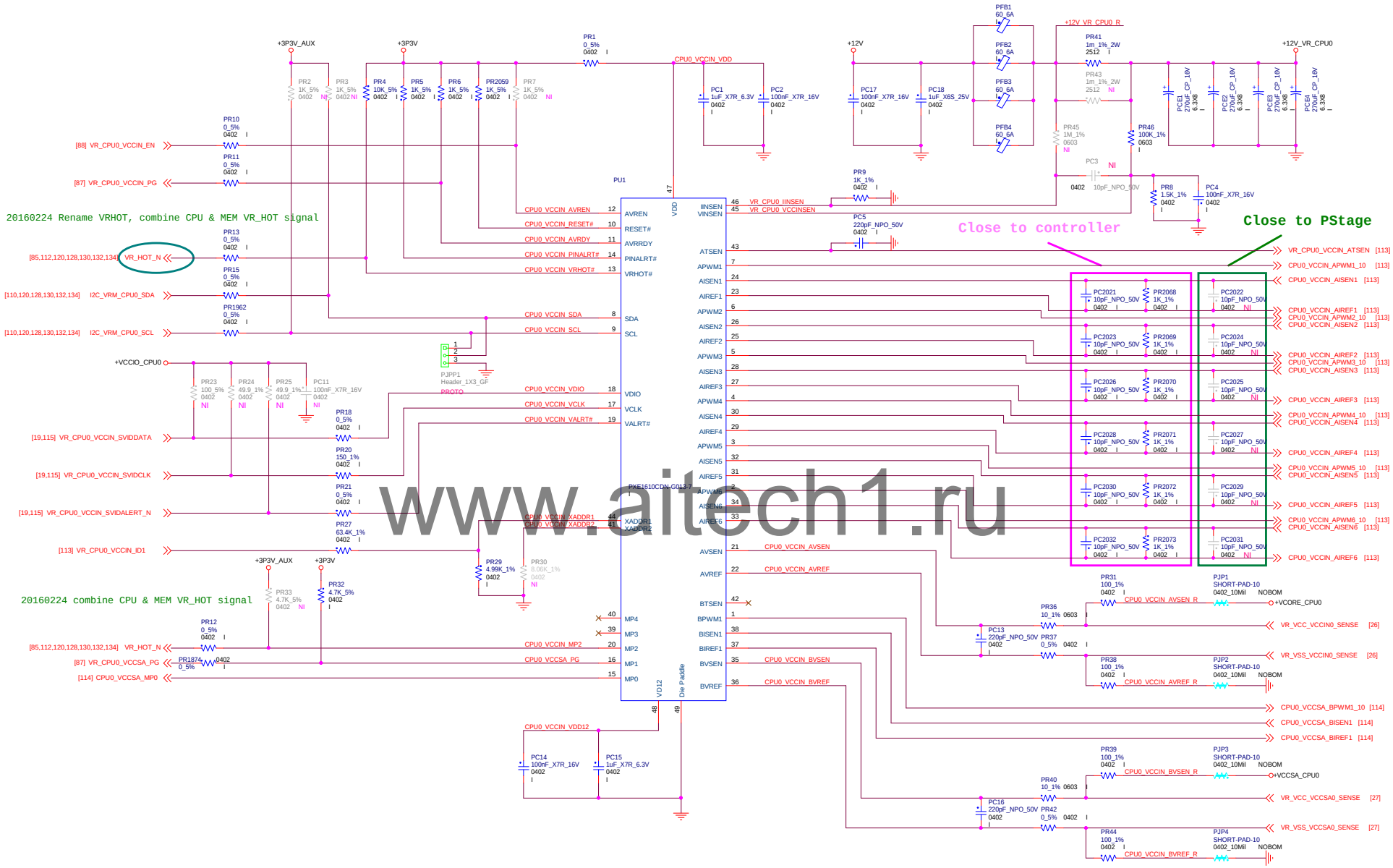
COMPASSED IMAGE

+VCORE_CPU0_Controller

VCCIN/SA SVID Address:0,1
PMBus Address:0xC0



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TITLE	VR, CPU0 CORE CONTORLLER
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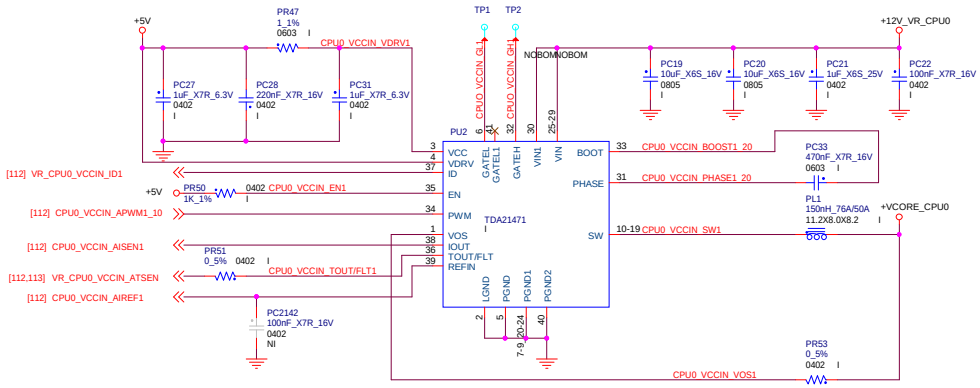
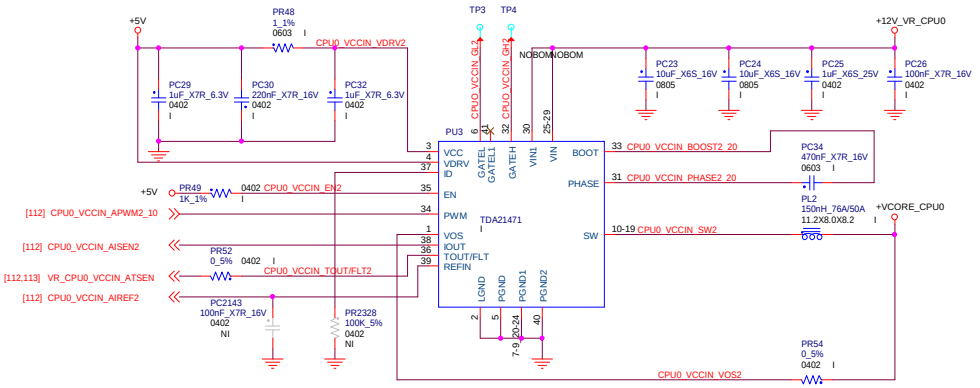
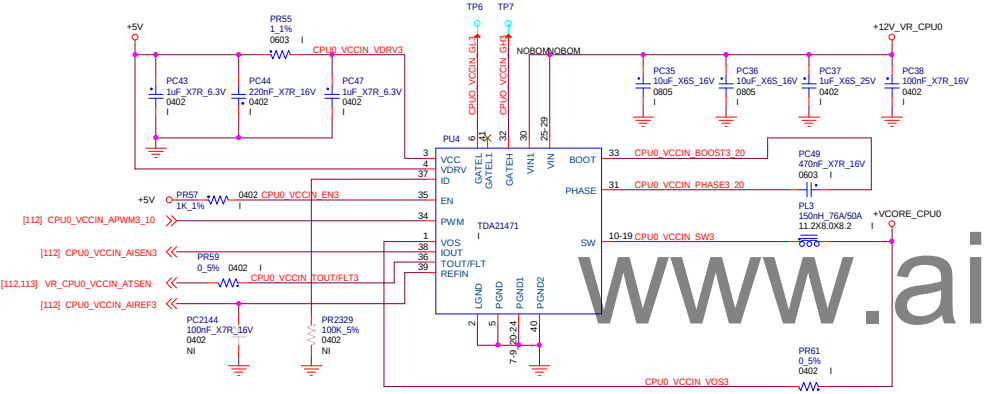
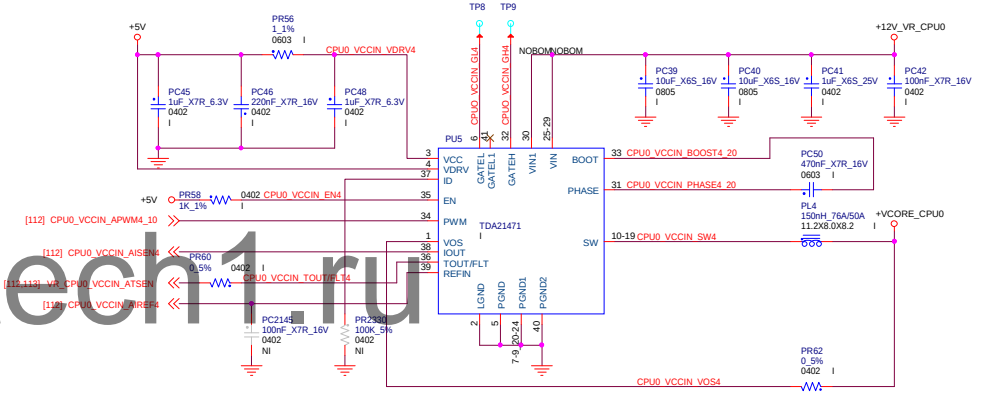
COMPRESSED IMAGE

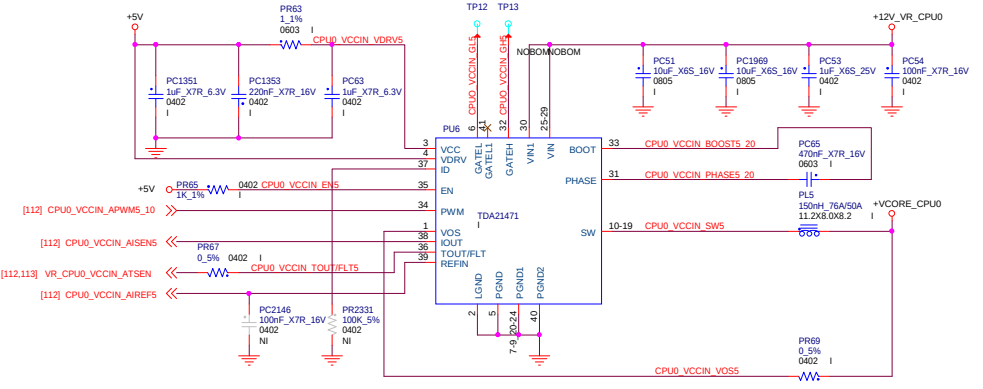
+VCORE_CPU0_Driver

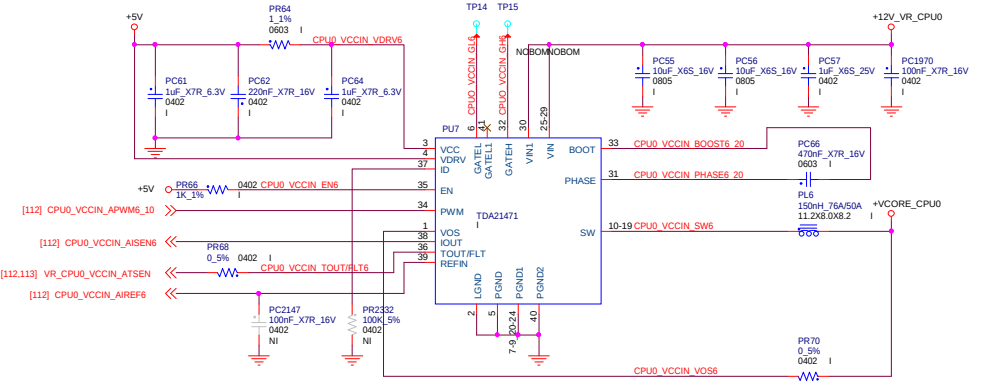












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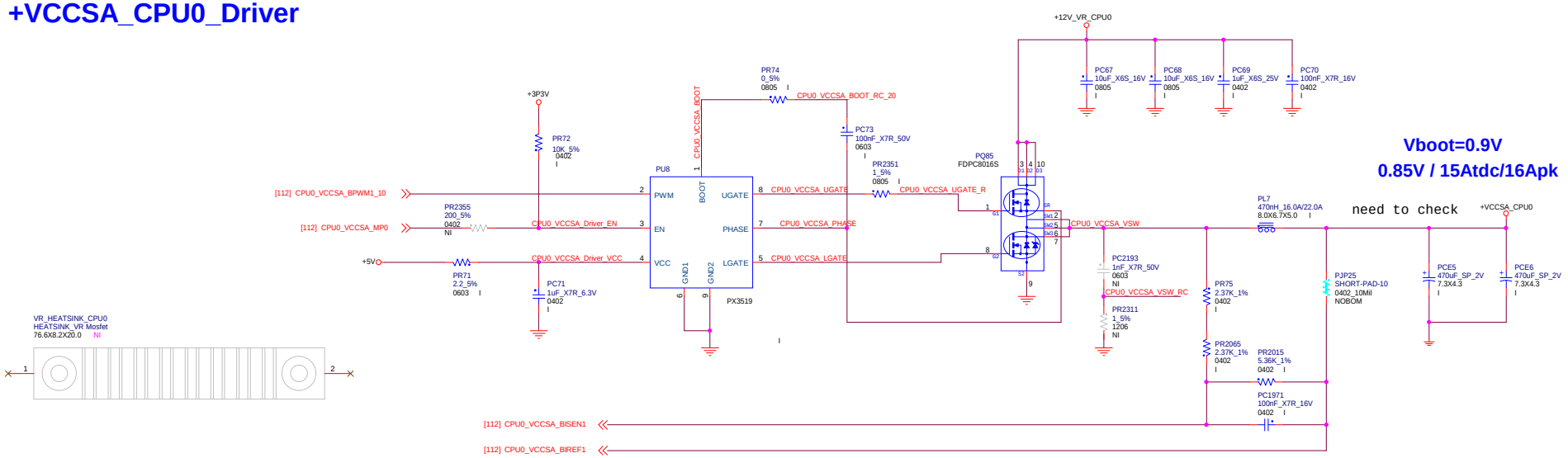
COMPRESSED IMAGE

+VCCSA_CPU0_Driver



Vboot=0.9V
0.85V / 15Atdc/16Apk

CPU0 VCCIN CAP

+1.8V / 89Atdc/228Apk
Vboot=1.7V

Bulk Caps x7

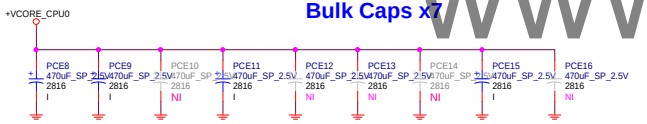
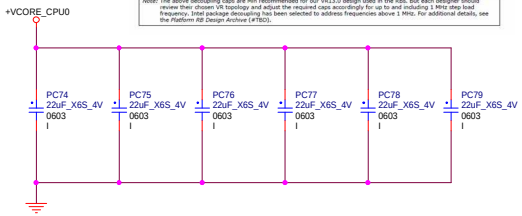
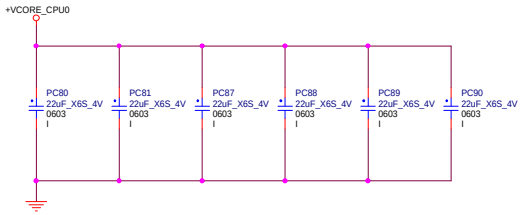


Table 204. CPU VccIN VR13.0 Recommended Output Caps per Socket, Based on Lightning Ridge RB Design

Cap Description	Min Quantity	Notes
470 µF / 2.5V / 20% / Alum / 3018	7	Bulk caps, place close to VR's output inductor's pads (2 top layer, 5 bottom layer)
22 µF / 4V / 20% / X6S / 0805	12	place close to the inductor pad (4 top layer, 8 bottom layer)
	40	place in the socket cavity (bottom layer)
10 µF / 6.3V / 20% / X6S / 0603	45	place in the socket cavity (top layer)

Note: The above decoupling caps are Min recommended for our VR13.0 design used in the RBs. But each designer should review their chosen VR topology and adjust the required caps accordingly for up to and including 1 MHz step load frequency. Intel package decoupling has been selected to address frequencies above 1 MHz. For additional details, see the Platform RB Design Archive (#TBD).





CPU0 VCCSA CAP

Place 4 VR output inductor

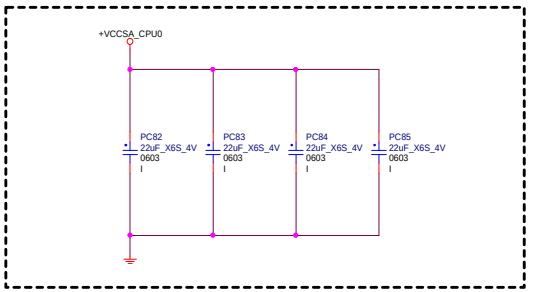


Table 211. PVCCSA VR Bulk / Decoupling Caps Based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 µF / 2.5V / 20% / Alum / 3018	2	bulk, place close to VR output inductor (Top layer)
22.0 µF / 4V / 10% / X6S / 0805	5	place 2 VR output inductor (Top layer) and 3 at socket cavity (Bottom layer)
10.0 µF / 6.3V / 10% / X6S / 0603	4	place all at Top Layer at socket cavity

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TITLE	VR, CPU0 VCCSA DRIVER
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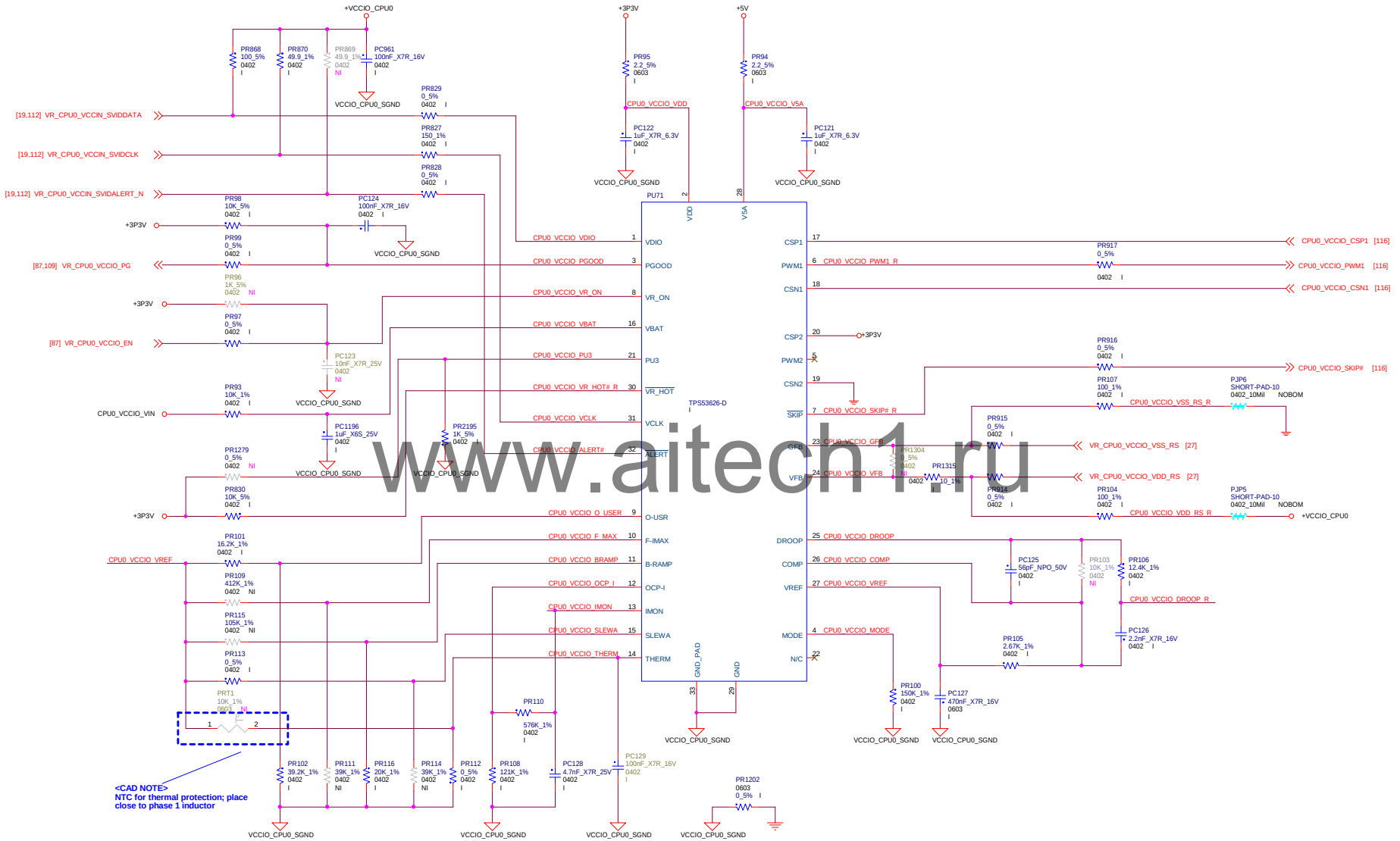
COMPRESSED IMAGE

+VCCIO_CPU0_Controller

CPU0
VCCIO SVID Bus= 02h



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TITLE	VR, CPU0 VCCIO CONTROLLER
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COMPRESSED IMAGE

+VCCIO_CPU0_DRIVER

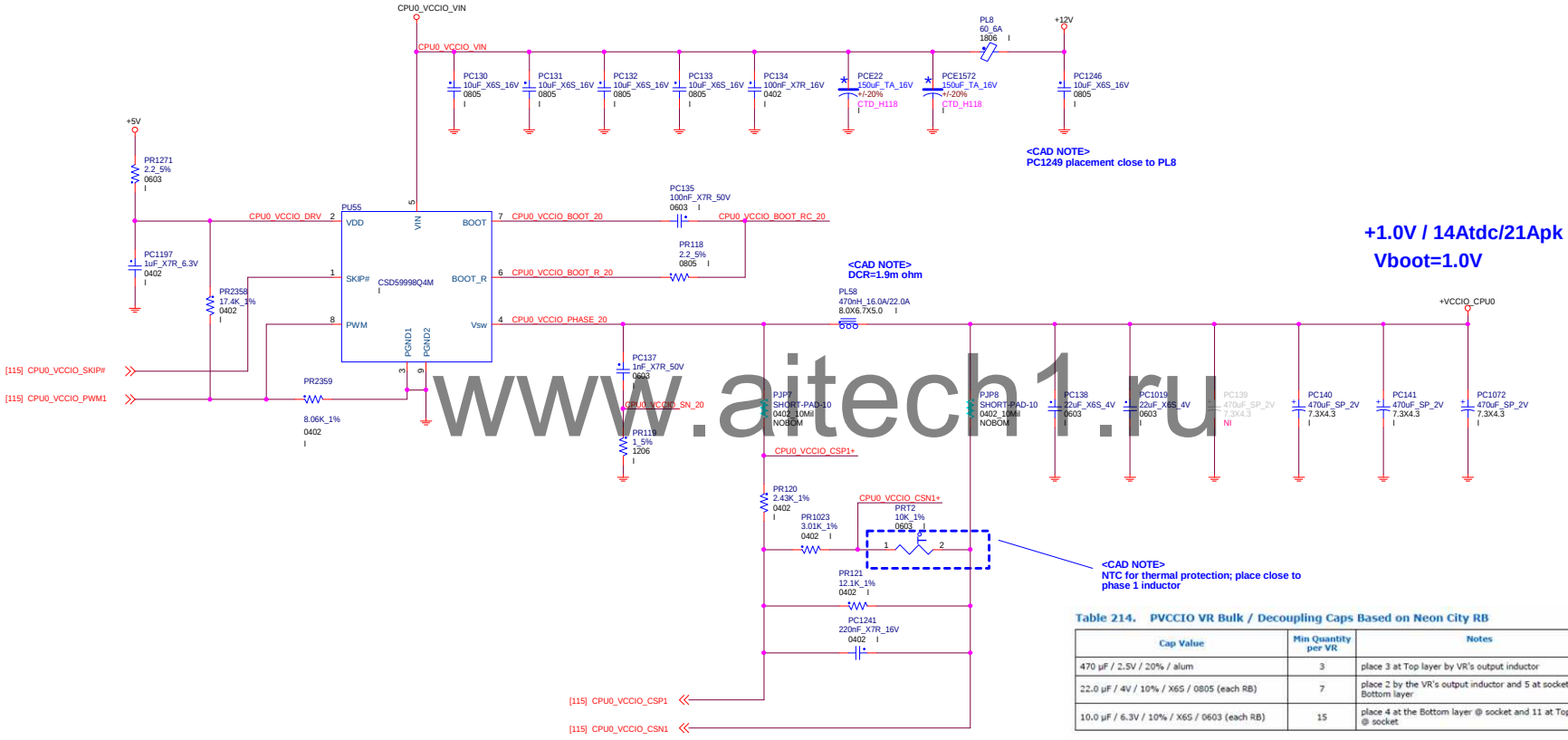

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Table 214. PVCCIO VR Bulk / Decoupling Caps Based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 µF / 2.5V / 20% / alum	3	place 3 at Top layer by VR's output inductor
22.0 µF / 4V / 10% / X6S / 0805 (each RB)	7	place 2 by the VR's output inductor and 5 at socket cavity Bottom layer
10.0 µF / 6.3V / 10% / X6S / 0603 (each RB)	15	place 4 at the Bottom layer @ socket and 11 at Top layer @ socket

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COMPRESSED IMAGE

+VMCP_CPU0_Controller (EMPTY)

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TITLE	VR, CPU0 VMCP CONTROLLER (EMPTY)		
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COMPRESSED IMAGE

+VMCP_CPU0_DRIVER(EMPTY)

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TITLE	VR, CPU0 VMCP DRIVER (EMPTY)		
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COMPRESSED IMAGE

+1V0_CPU0_Controller

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TITLE	VR. CPU0 1V0 CONTROLLER (EMPTY)
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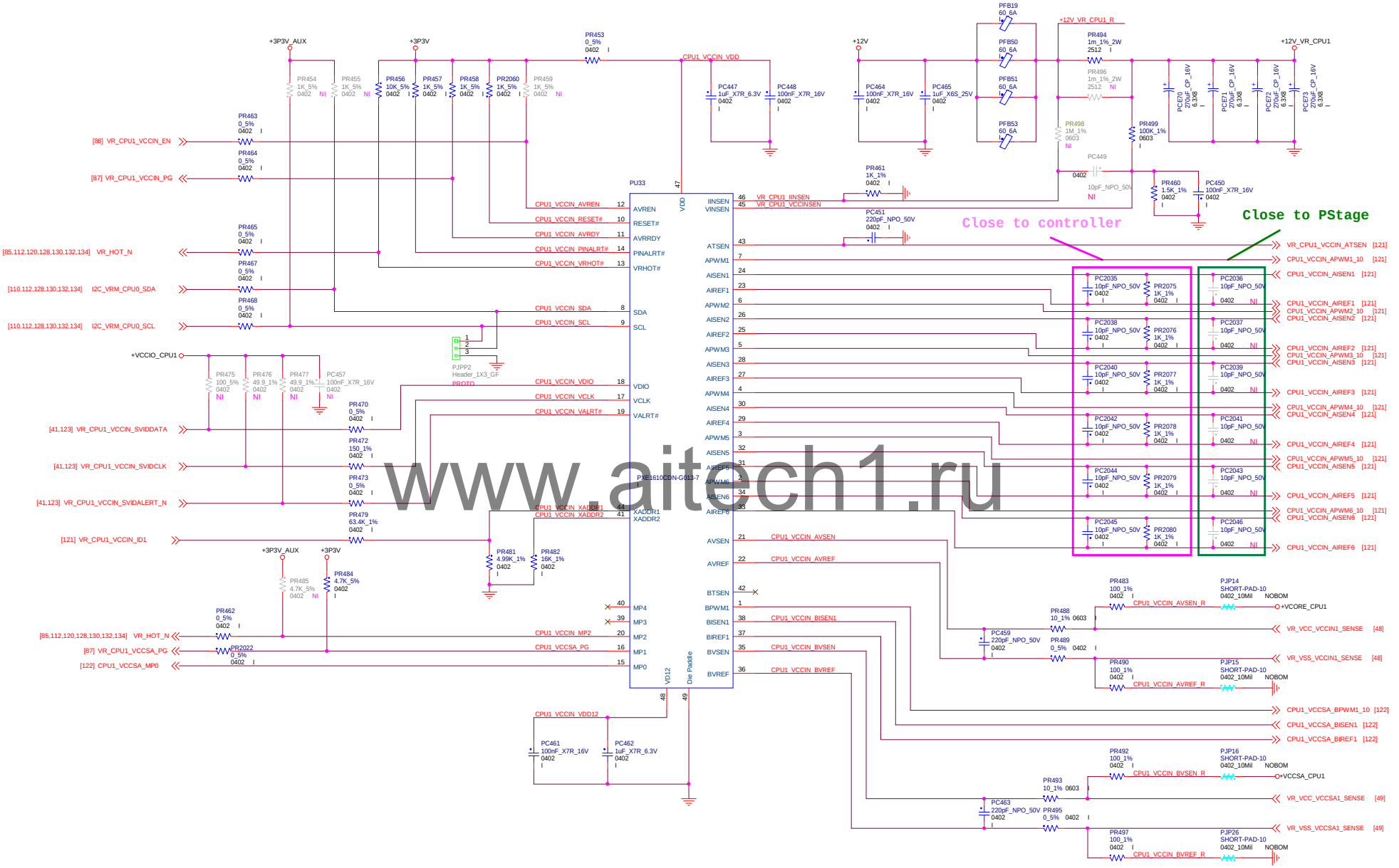
COMPRESSED IMAGE

+VCORE_CPU1_Controller

VCCIN/SA SVID Address:0,1
PMBus Address:0xC4



TITLE	VR, CPU1 CORE CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
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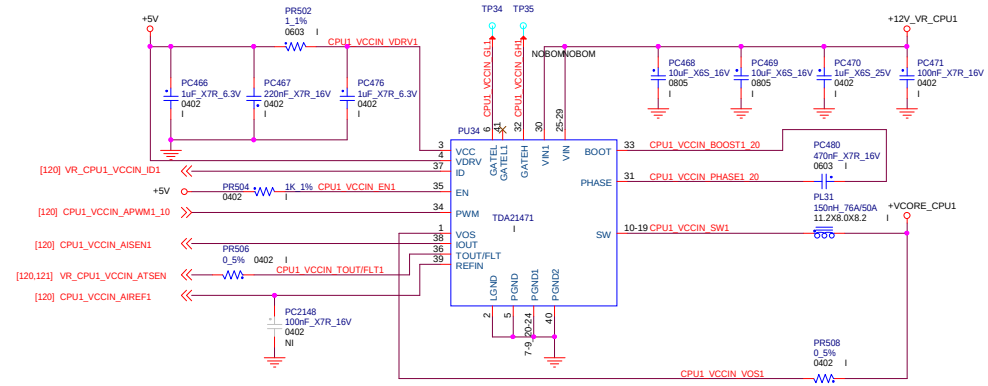
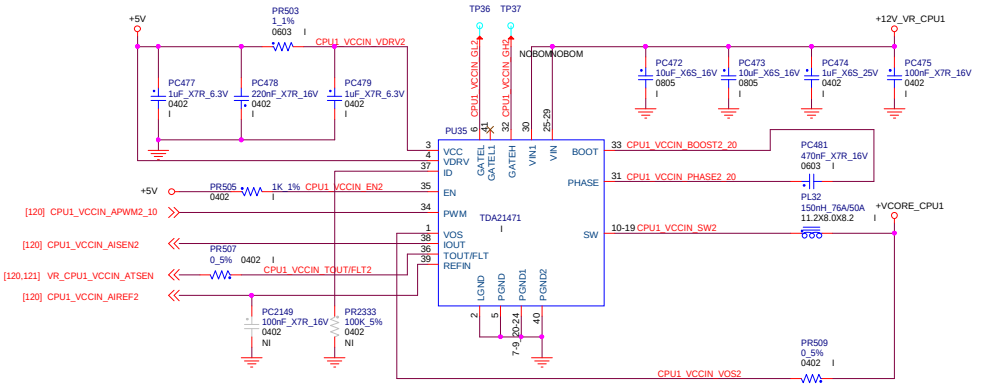
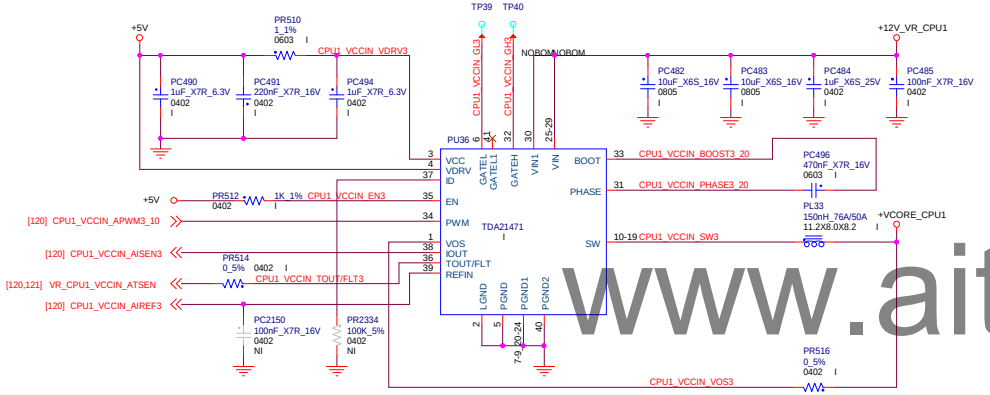
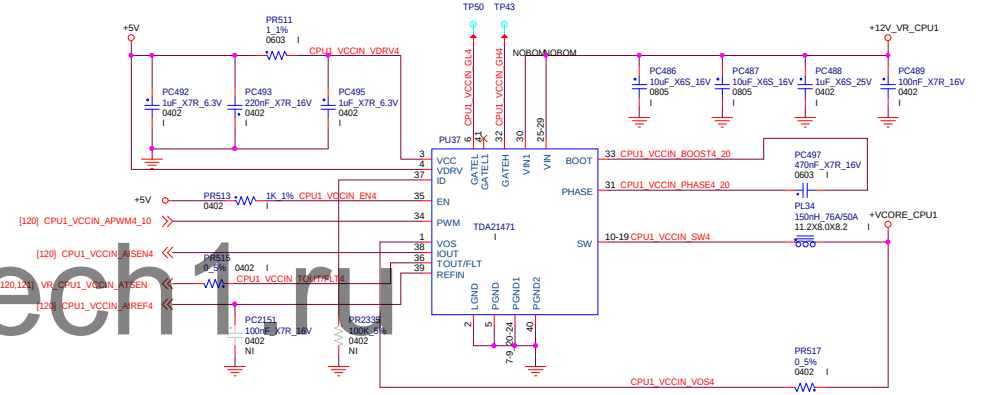
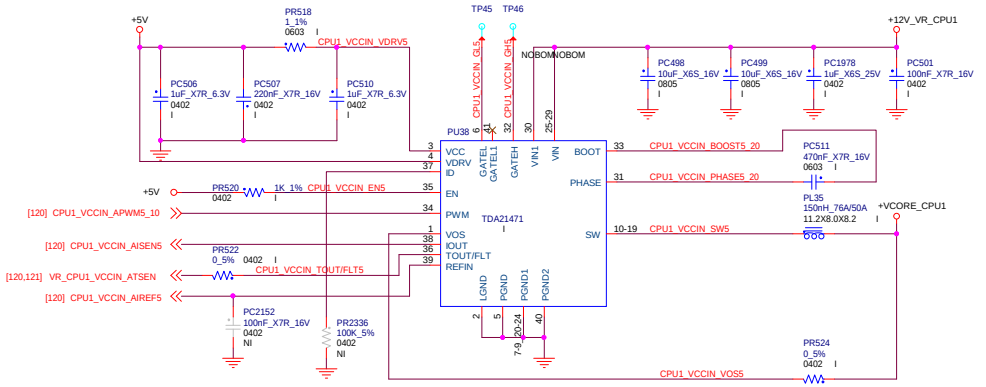
+VCORE_CPU1_Driver

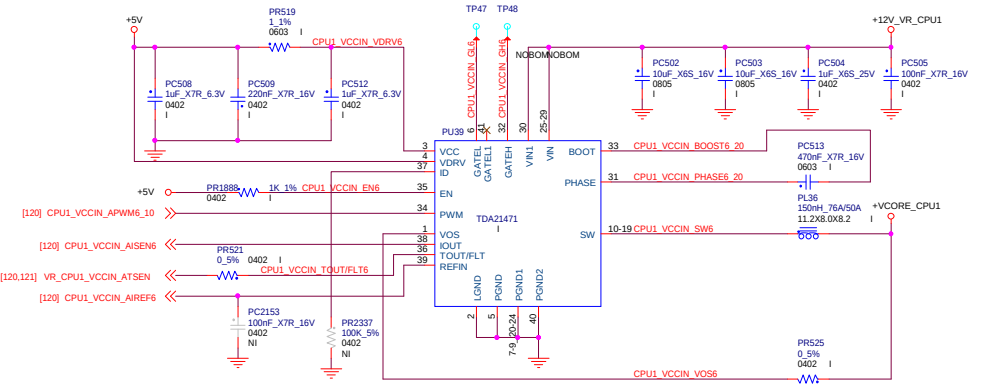












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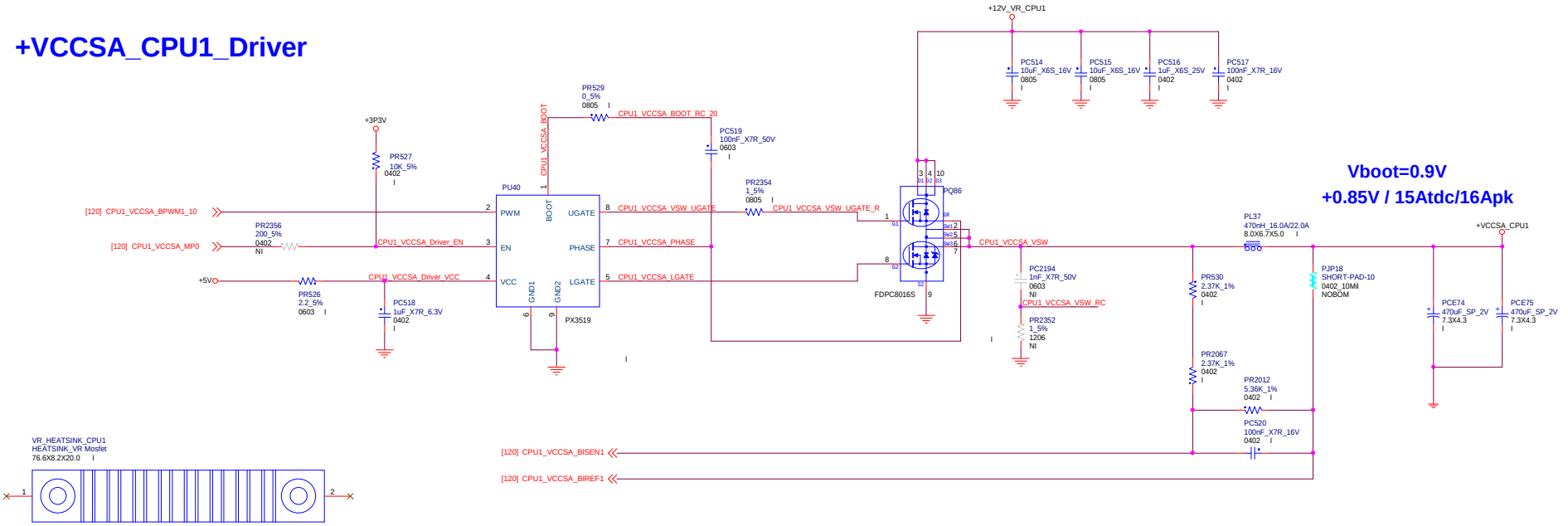
COMPRESSED IMAGE

+VCCSA_CPU1_Driver



CPU1 VCCIN CAP

+1.8V / 89Atdc/228Apk
Vboot=1.7V

Bulk Caps x7

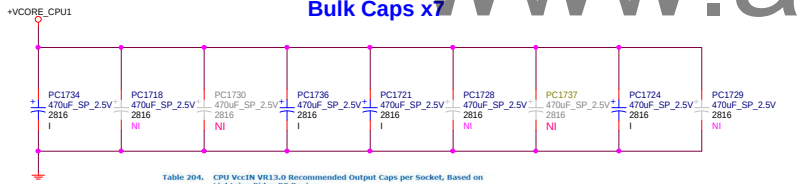
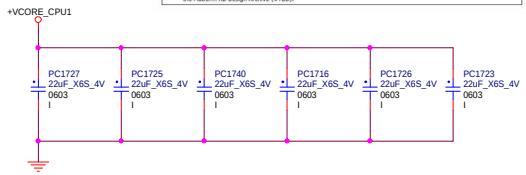
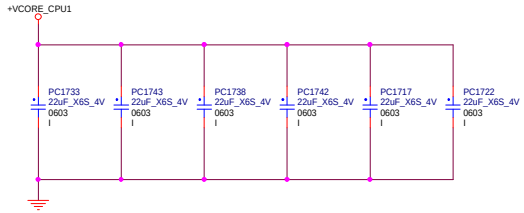


Table 204. CPU VccIN VR13.0 Recommended Output Caps per Socket, Based on Lightning Ridge RB Design

Cap Description	Min Quantity	Notes
470 µF / 2.5V / 20% / Alum / 3018	7	Bulk caps, place close to VR's output inductor's pads (2 top layer, 5 bottom layer)
22 µF / 4V / 20% / X6S / 0805	12	place close to the inductor pad (4 top layer, 8 bottom layer)
	40	place in the socket cavity (bottom layer)
10 µF / 6.3V / 20% / X6S / 0603	45	place in the socket cavity (top layer)

Note: The above decoupling caps are Min recommended for our VR13.0 design used in the RBs. But each designer should review their chosen VR topology and adjust the required caps accordingly for up to and including 1 MHz step load frequency. Intel package decoupling has been selected to address frequencies above 1 MHz. For additional details, see the *Platform RB Design Archive* (#TBD).





CPU1 VCCSA CAP

Place 4 VR output inductor

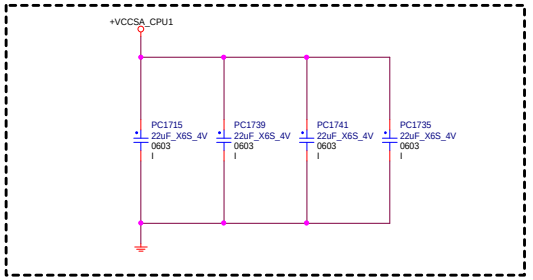


Table 211. PVCCSA VR Bulk / Decoupling Caps Based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 µF / 2.5V / 20% / Alum / 3018	2	bulk, place close to VR output inductor (Top layer)
22.0 µF / 4V / 10% / X6S / 0805	5	place 2 VR output inductor (Top layer) and 3 at socket cavity (Bottom layer)
10.0 µF / 6.3V / 10% / X6S / 0603	4	place all at Top Layer at socket cavity

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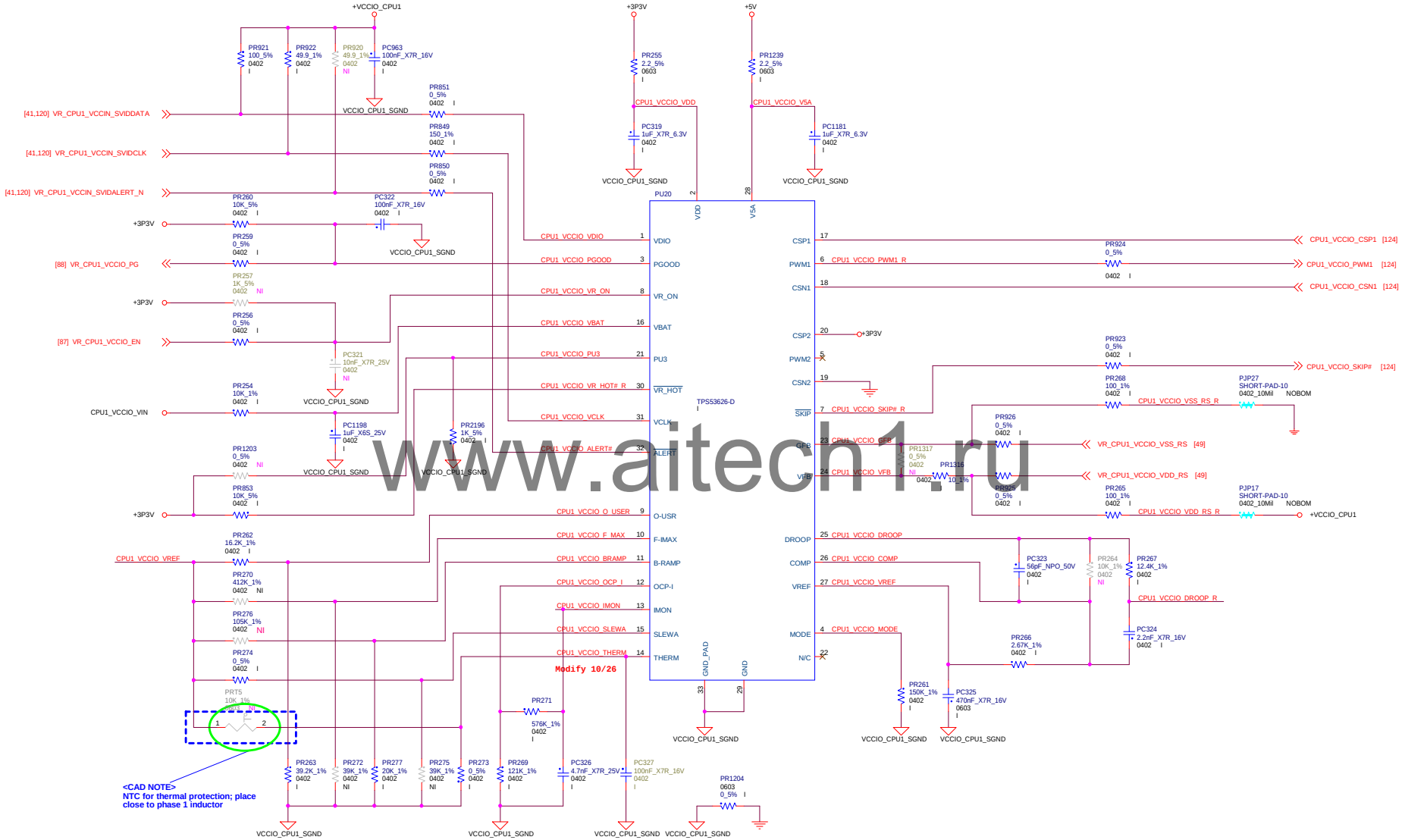
TITLE	VR, CPU1 VCCSA DRIVER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	122 of 150

COMPRESSED IMAGE

+VCCIO_CPU1_Controller

CPU1
VCCIO SVID Bus= 02h



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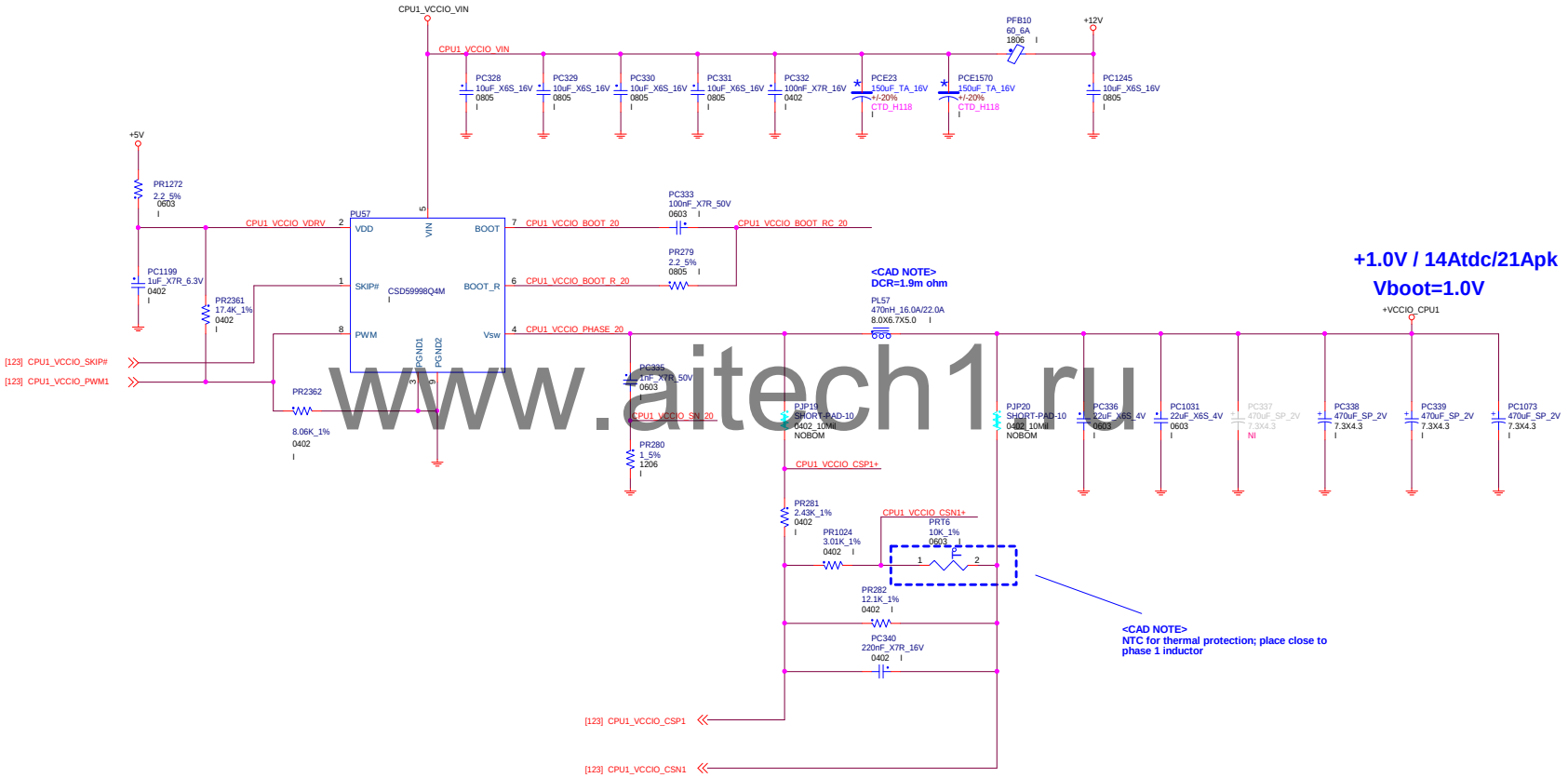
TITLE	VR, CPU1 VCCIO CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	123 of 150

COMPRESSED IMAGE

+VCCIO_CPU1_DRIVER



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TITLE	VR, CPU1 VCCIO DRIVER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	124 of 150

COMPRESSED IMAGE

+VMCP_CPU1_Controller(EMPTY)

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TITLE	VR, CPU1 VMCP CONTROLLER (EMPTY)
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	125 of 150

COMPRESSED IMAGE

+VMCP_CPU1_DRIVER(EMPTY)

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TITLE	VR, CPU1 VMCP DRIVER (EMPTY)		
DWG NO.	MATIRA 7	REV.	A00
DATE	Thursday, June 29, 2017	SHEET	126 of 150

COMPRESSED IMAGE

+1V0_CPU1_Controller

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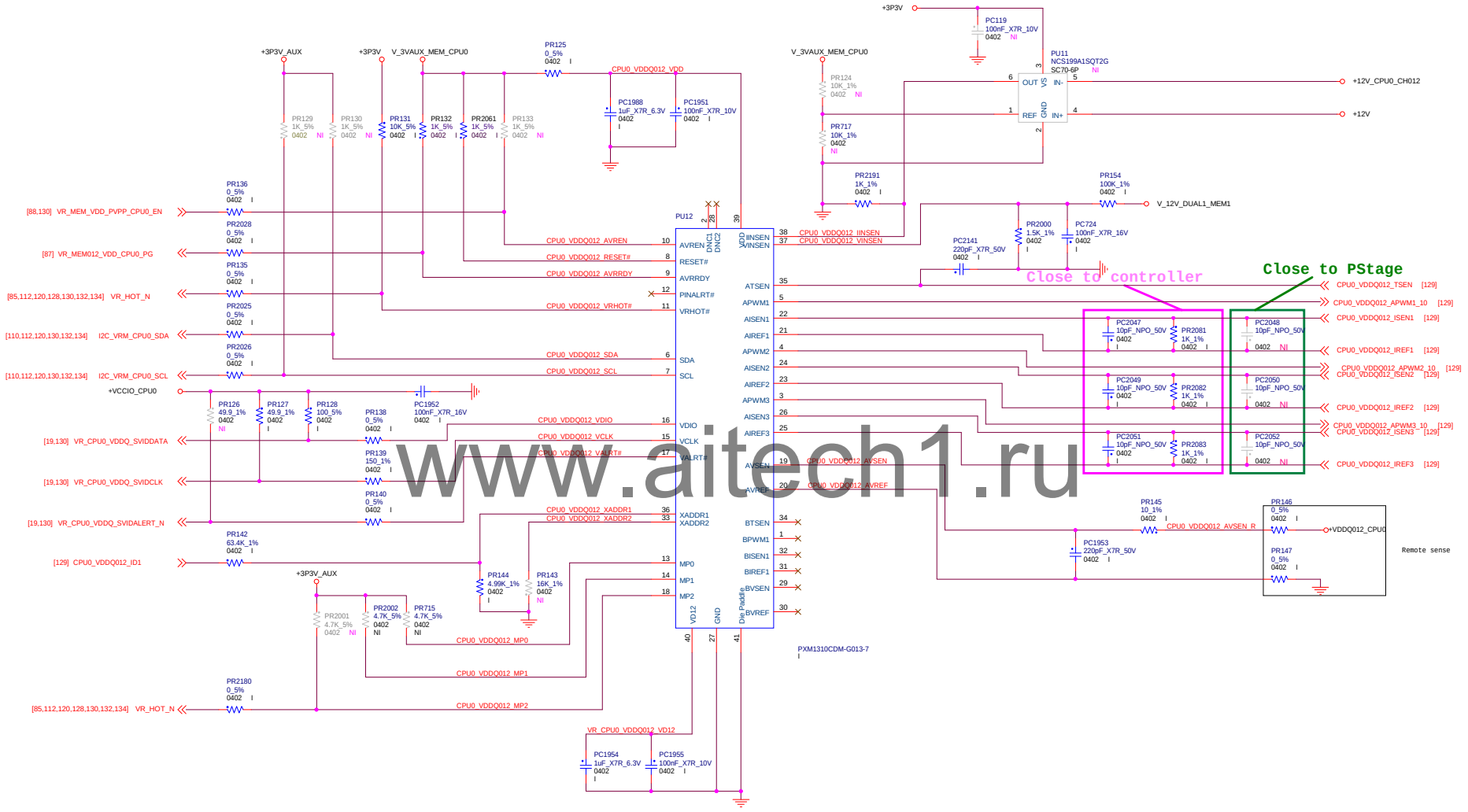
TITLE	VR. CPU1 1V0 CONTROLLER (EMPTY)
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	127 of 150

COMPRESSED IMAGE

+VDDQ012_CPU0_Controller

VDDQ SVID Address:0,2
PMBus Address:0xE0



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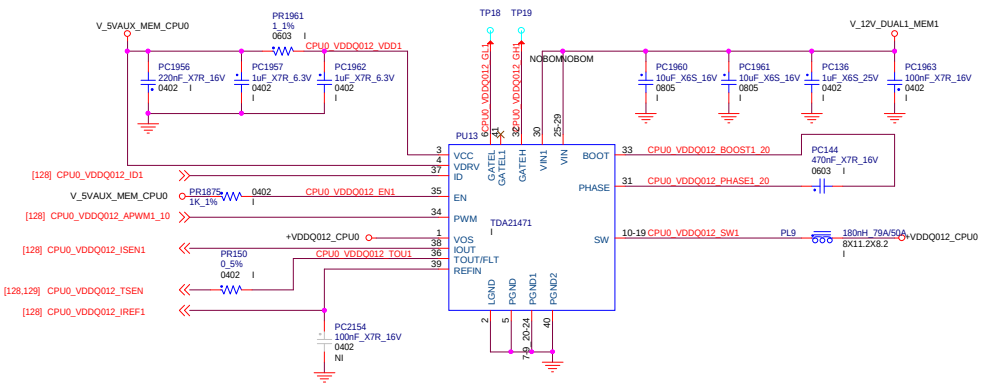
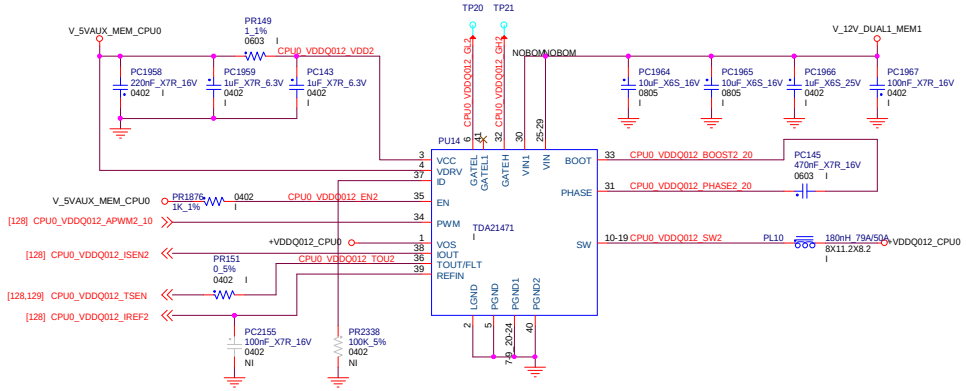
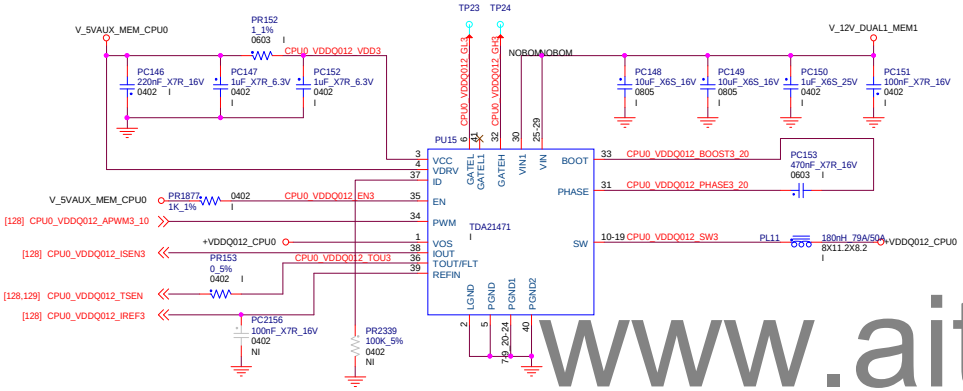
TITLE	VR, CPU0 DDR012 CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	128 of 150

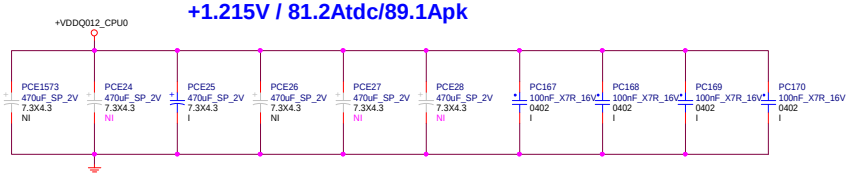
+VDDQ012_CPU0_Driver

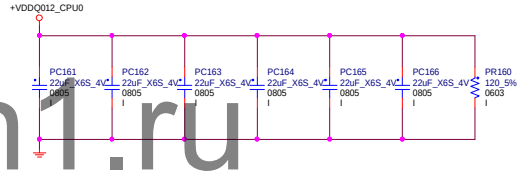






+1.215V / 81.2Atdc/89.1Apk





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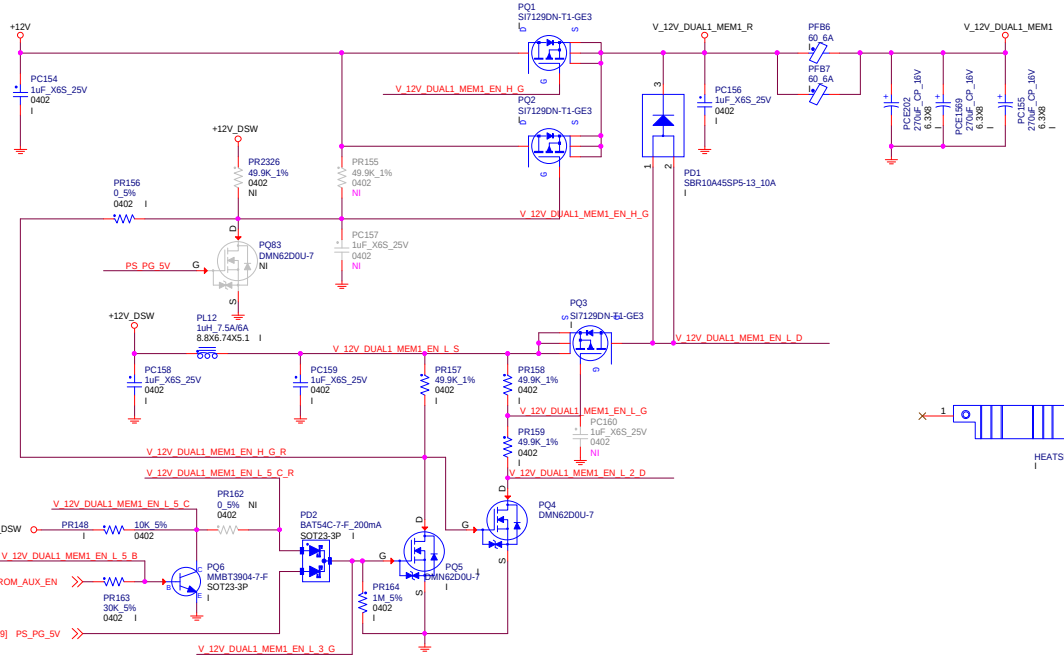

Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.

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TITLE	VR, CPU0 VDDQ012 DRIVER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	129 of 150

COMPRESSED IMAGE

+VDDQ345_CPU0_Controller

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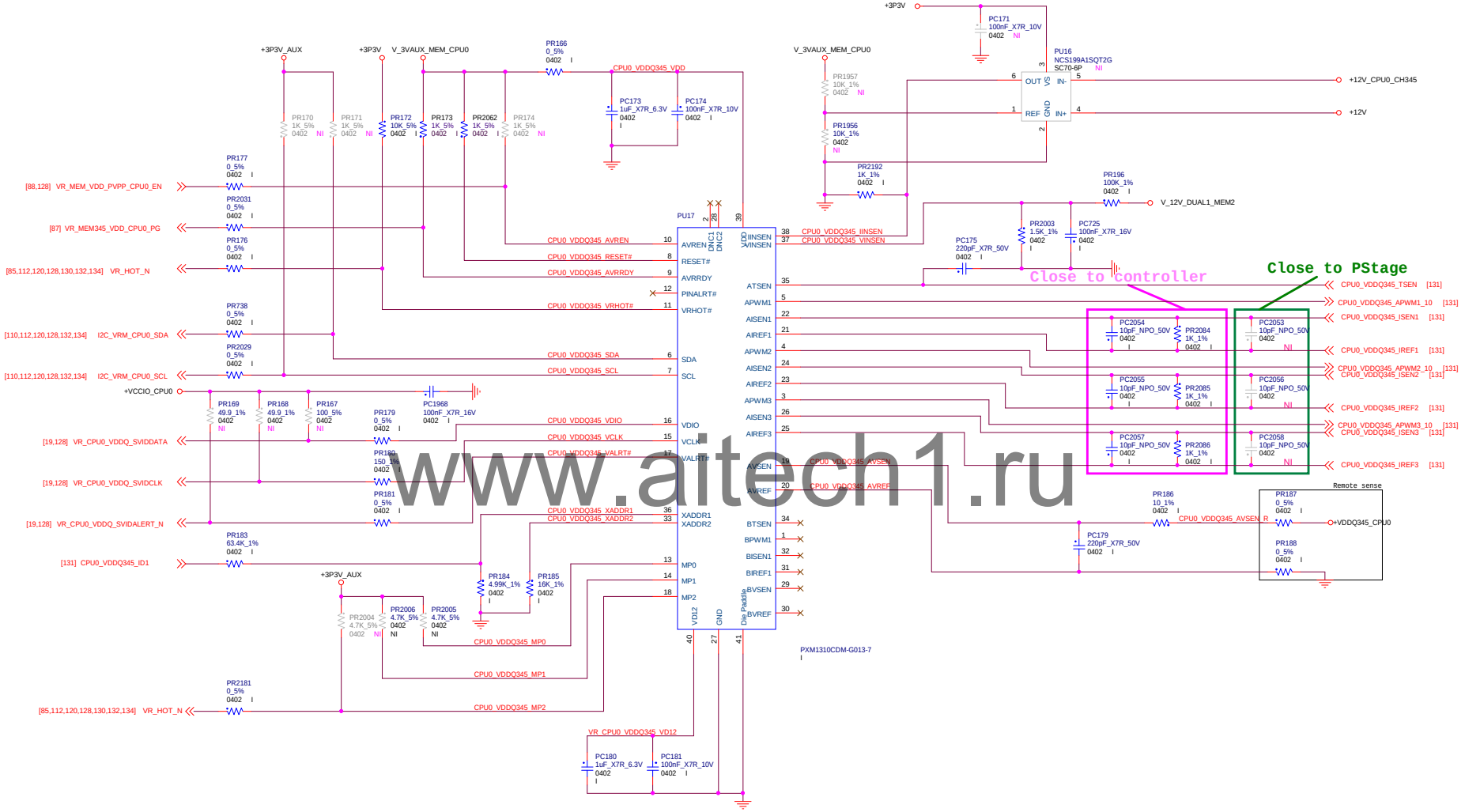
PMBus Address:0xE4



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TITLE	VR, CPU0 VDDQ345 CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	130 of 150

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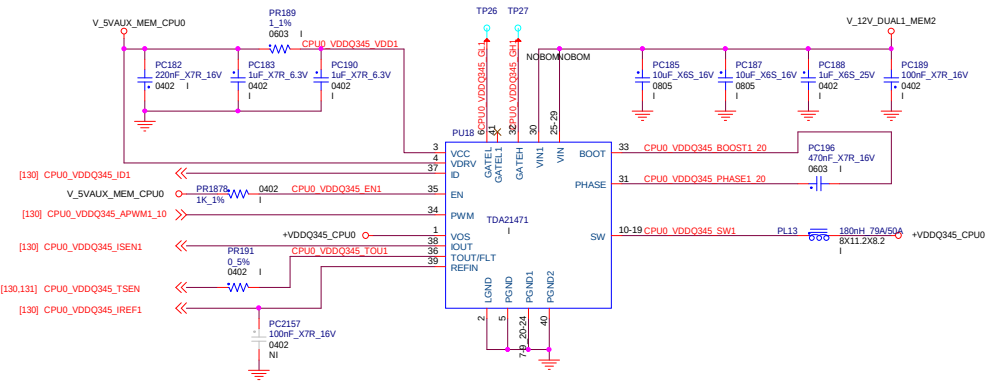
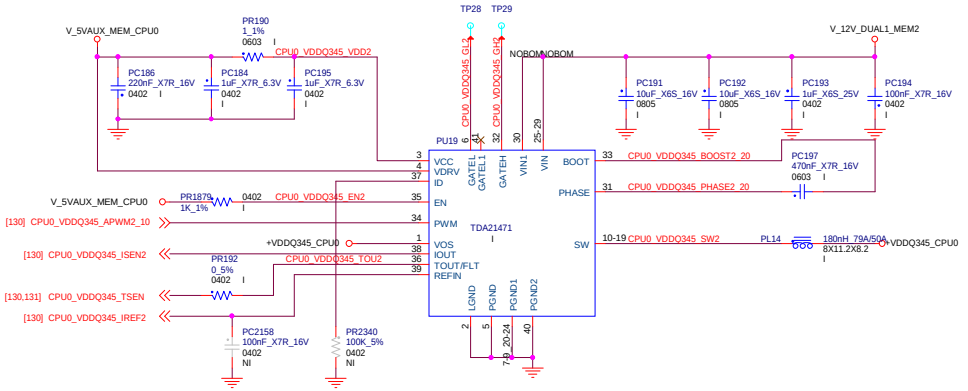
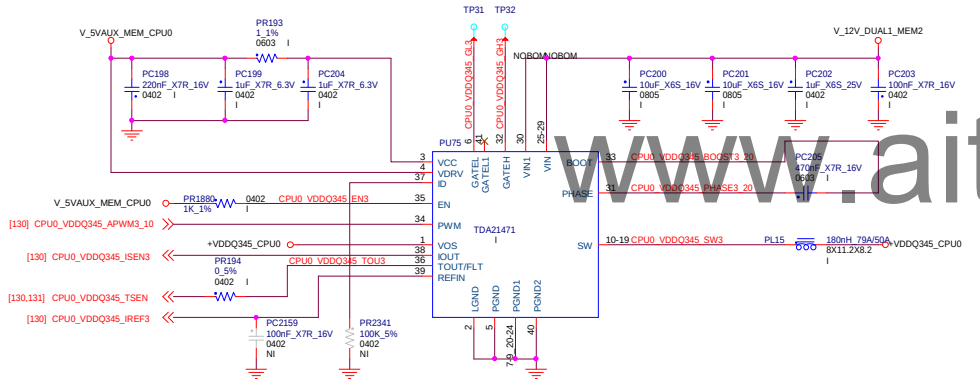
COMPRESSED IMAGE

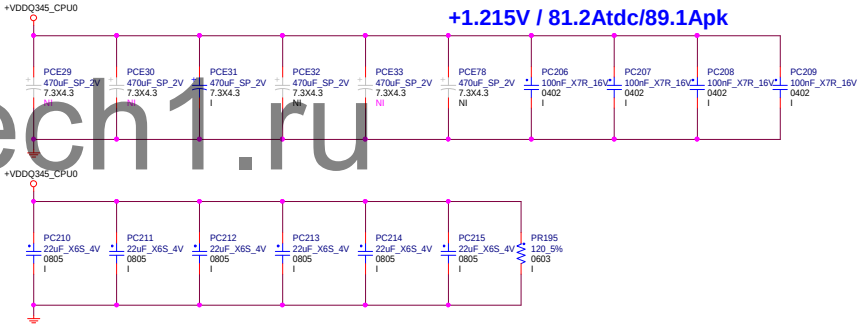
+VDDQ345_CPU0_Driver







+1.215V / 81.2Atdc/89.1Apk



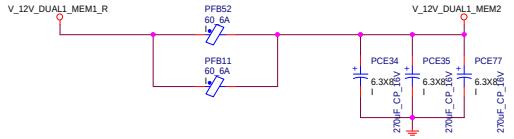


Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.

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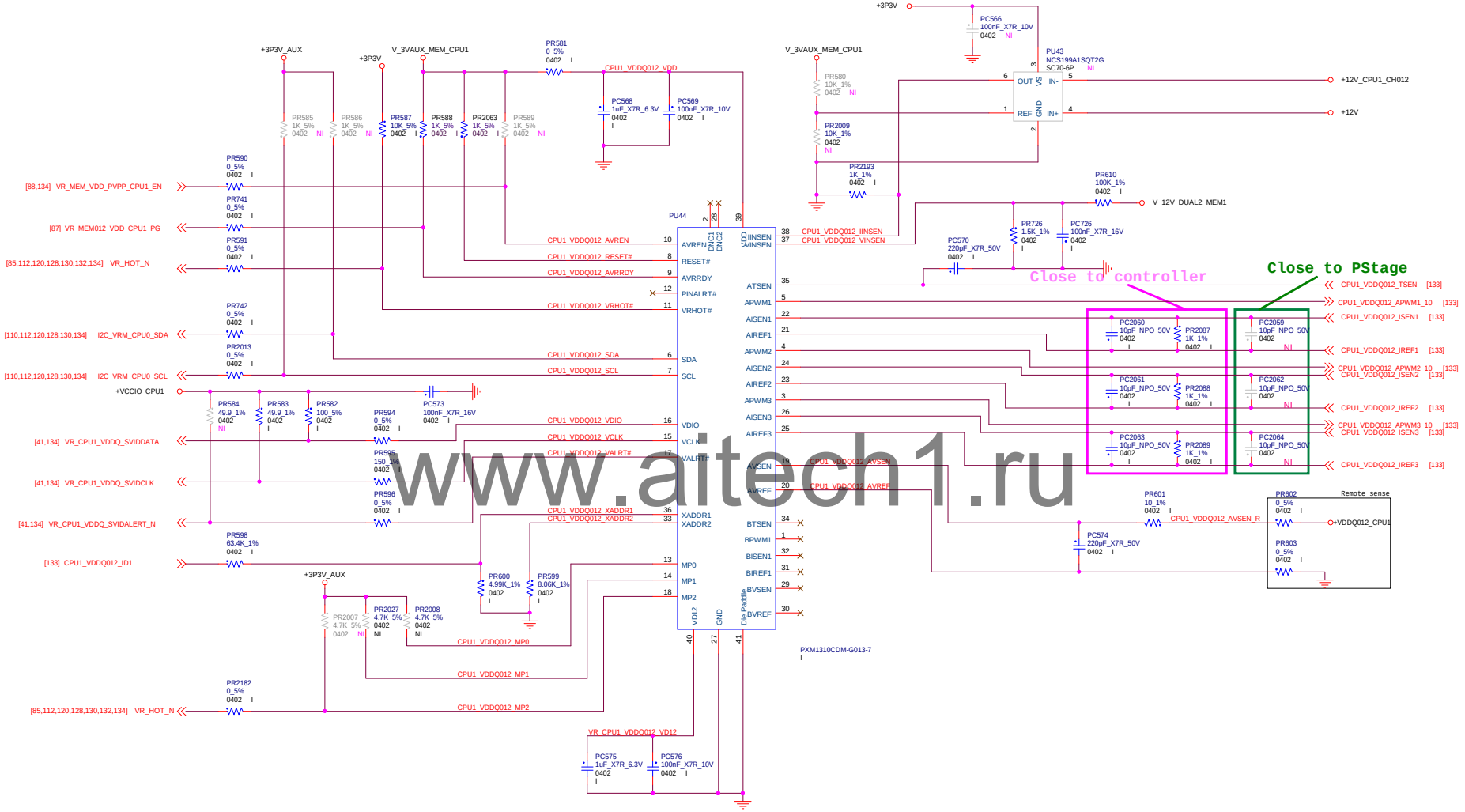
TITLE	VR, CPU0 VDDQ345 DRIVER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	131 of 150

COMPRESSED IMAGE

+VDDQ012_CPU1_Controller

VDDQ SVID Address:0,2
PMBus Address:0xE8



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TITLE	VR, CPU1 VDDQ012 CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	132 of 150

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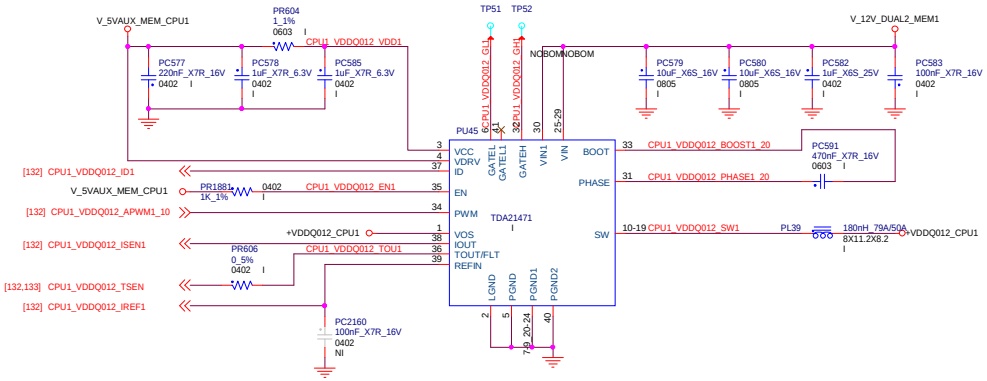
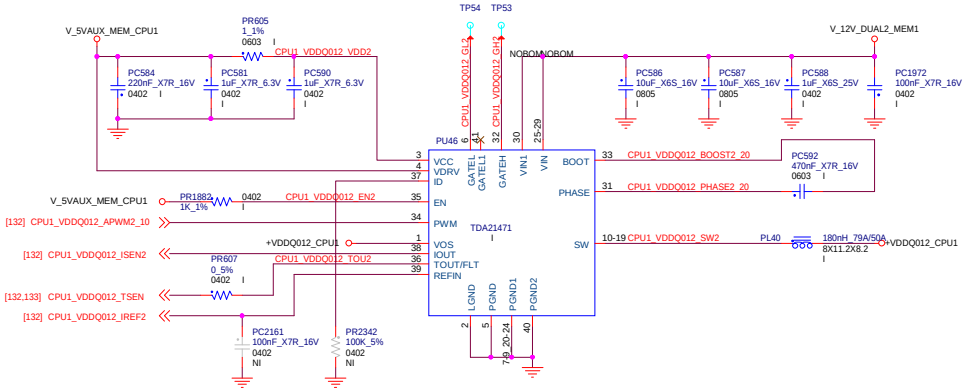
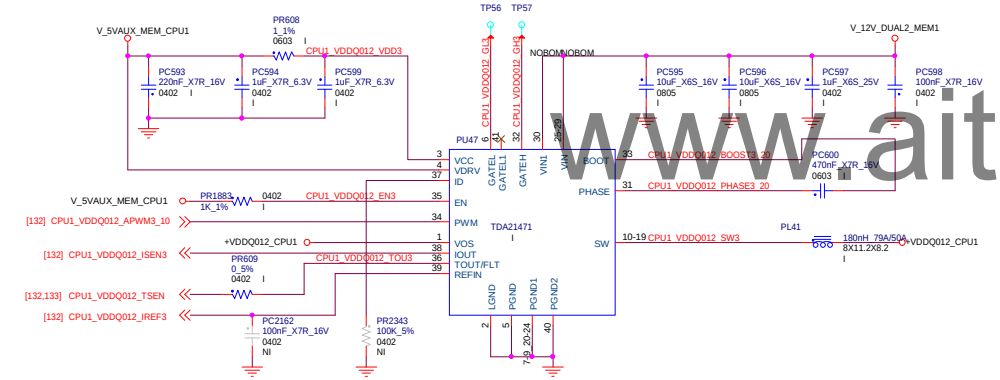
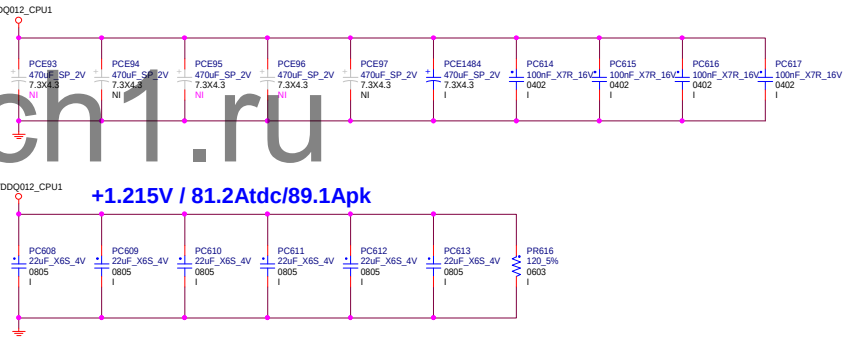
COMPRESSED IMAGE

+VDDQ012_CPU1_Driver









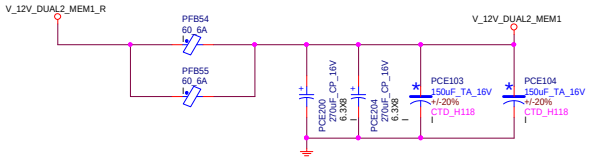


Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.

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TITLE	VR, CPU1 VDDQ012 DRIVER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
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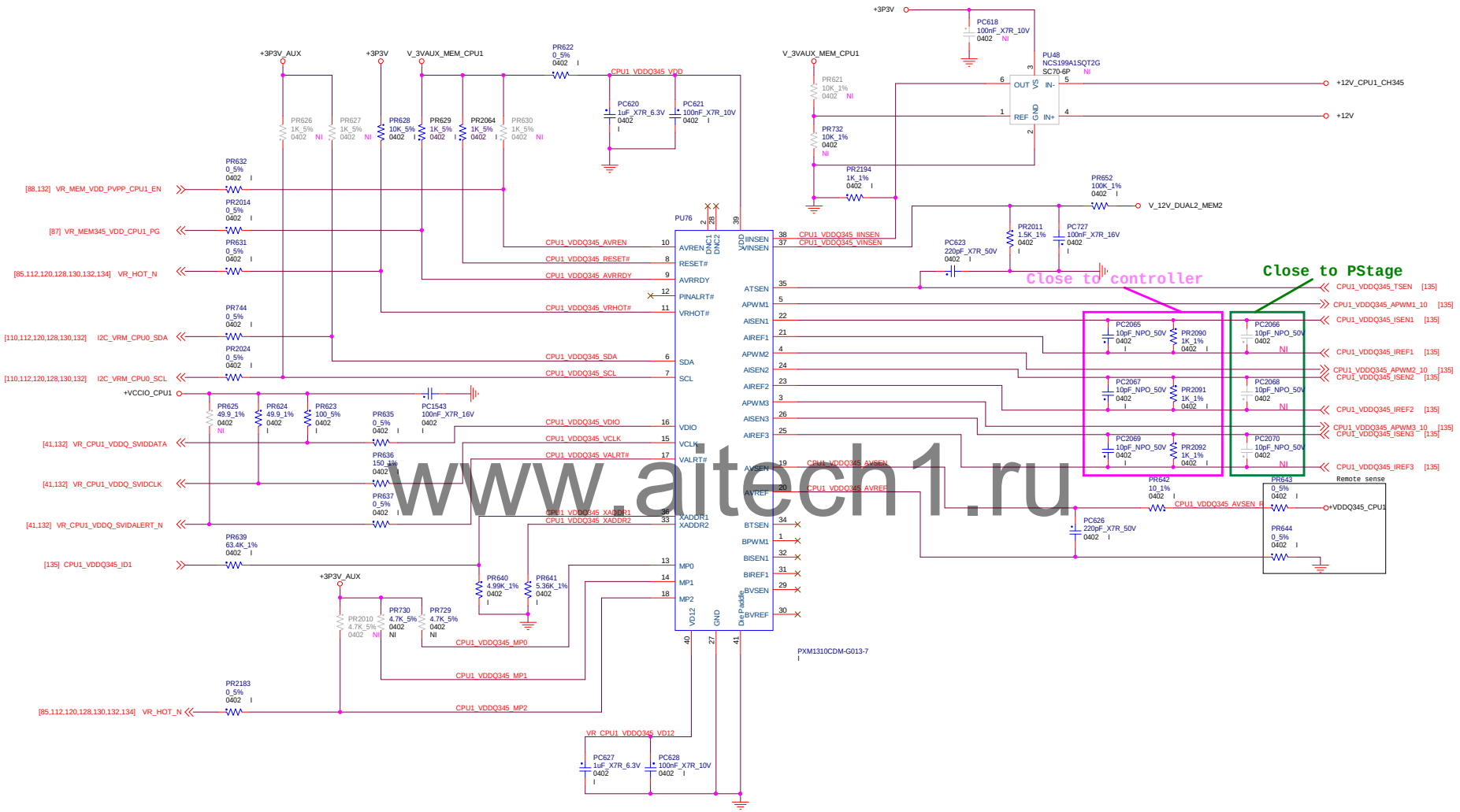
COMPRESSED IMAGE

+VDDQ345_CPU1_Controller

VDDQ SVID Address:0,2
PMBus Address:0xEC



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TITLE	VR, CPU1 VDDQ0345 CONTROLLER
DWG NO.	MATIRA 7
REV.	A00
DATE	Thursday, June 29, 2017
SHEET	134 of 150

+VDDQ345_CPU1_Driver

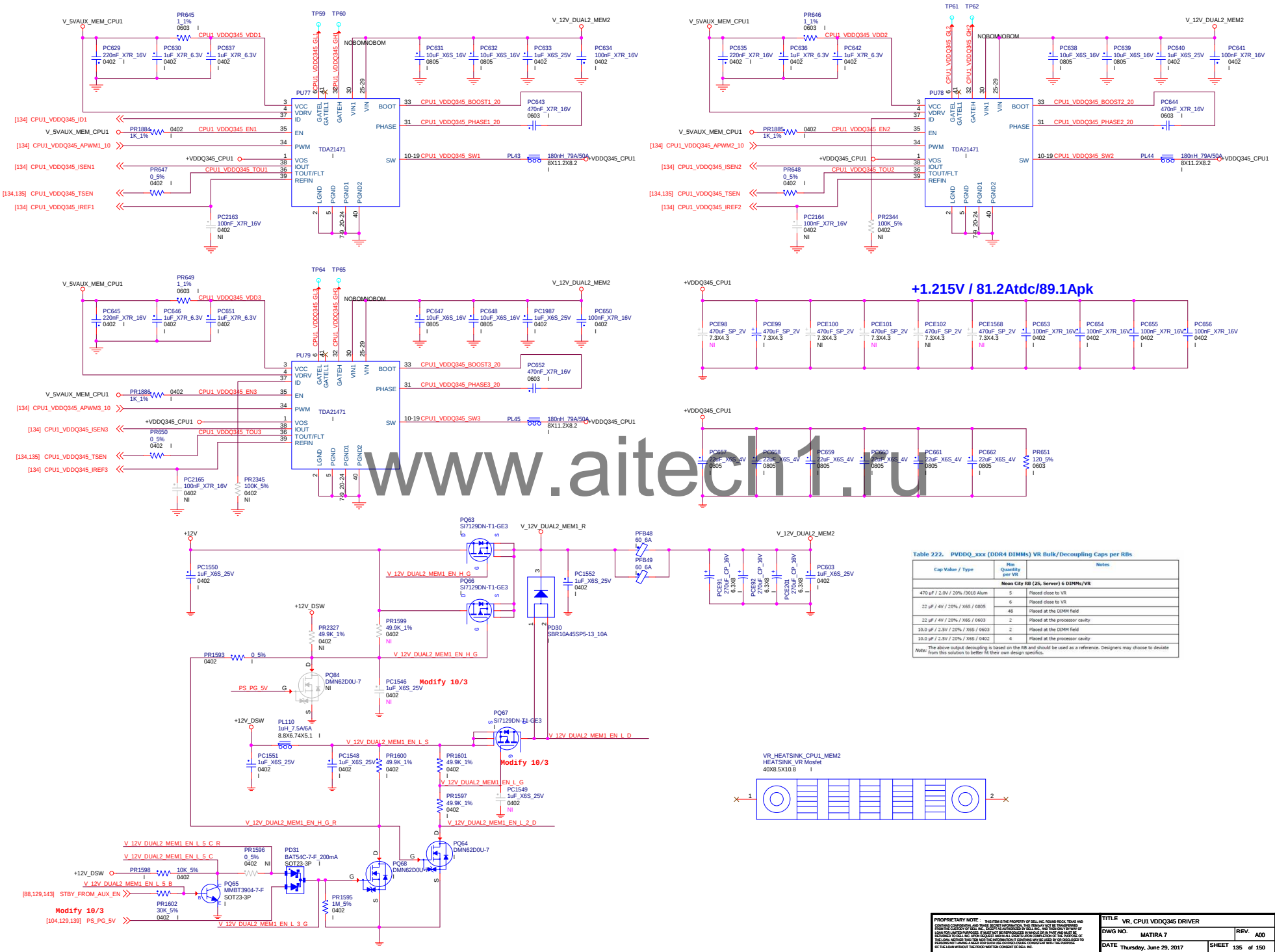

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Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.

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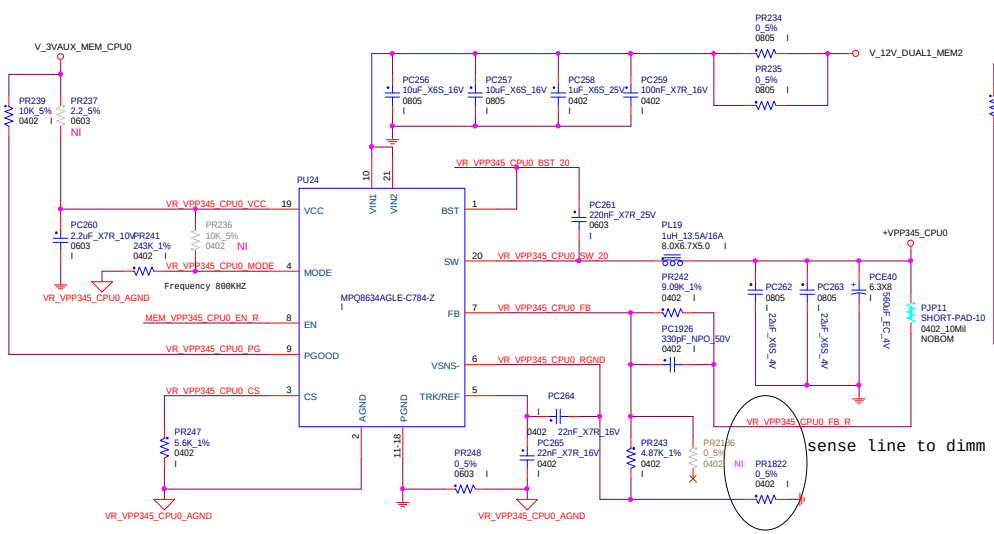
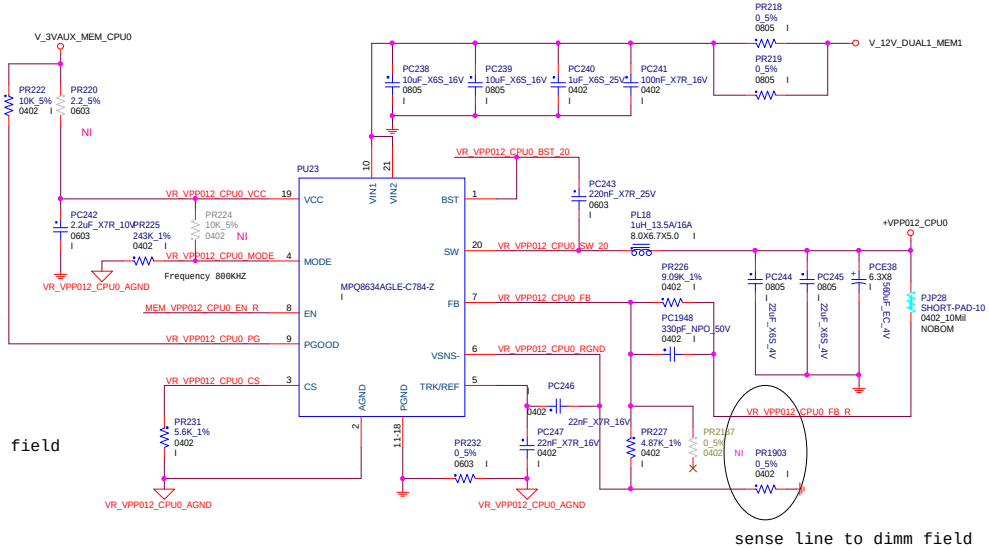
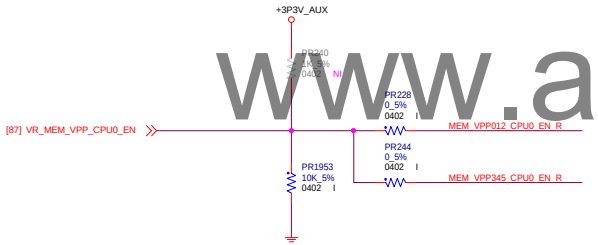
COMPRESSED IMAGE

CPU0 MEM VPP







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+2.575V / 6.77Atdc/8.922Apk

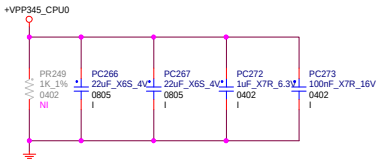

Table 227. PVPP_xxx VR Bulk / Decoupling Caps, per Neon City RB

Cap Value	Min Quantity per VR	Notes
RB (2S, Server) 6 DIMMs / VR		
560 µF / 4V / 10% / Alum THMT	1	Bulk, place close to VR output inductor
Cap Value	**Min Quantity per VR**	**Notes**
22.0 µF / 4V / 20% / X6S / 0805	6	Place 2 close to VR output inductor (bottom), 4 between DIMMs (top)
10.0 µF / 4V / 20% / X6S / 0603	8	Place between DIMMs, 2 caps/DIMM

Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.

+2.575V / 6.77Atdc/8.922Apk

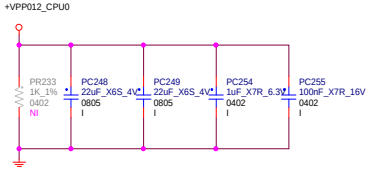

Table 227. PVPP_xxx VR Bulk / Decoupling Caps, per Neon City RB

Cap Value	Min Quantity per VR	Notes
RB (2S, Server) 6 DIMMs / VR		
560 µF / 4V / 10% / Alum THMT	1	Bulk, place close to VR output inductor
Cap Value	**Min Quantity per VR**	**Notes**
22.0 µF / 4V / 20% / X6S / 0805	6	Place 2 close to VR output inductor (bottom), 4 between DIMMs (top)
10.0 µF / 4V / 20% / X6S / 0603	8	Place between DIMMs, 2 caps/DIMM

Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.

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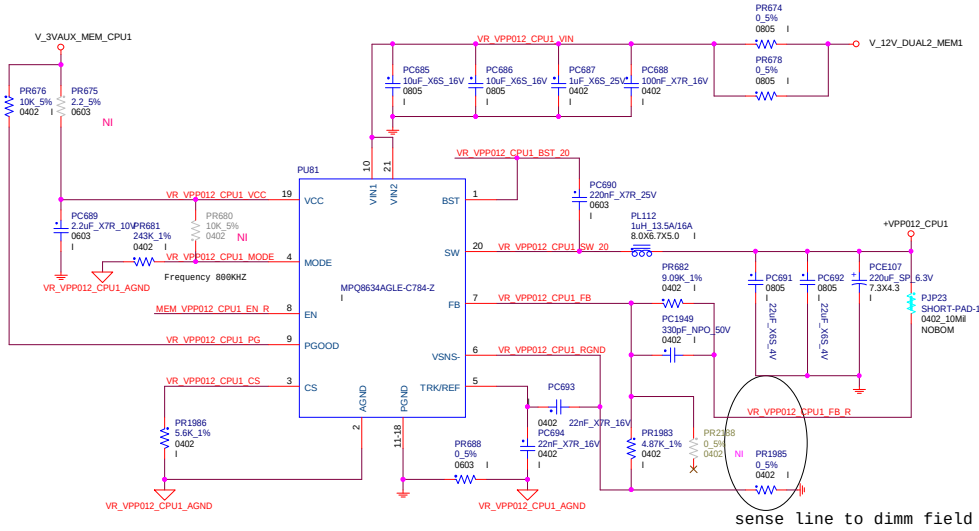
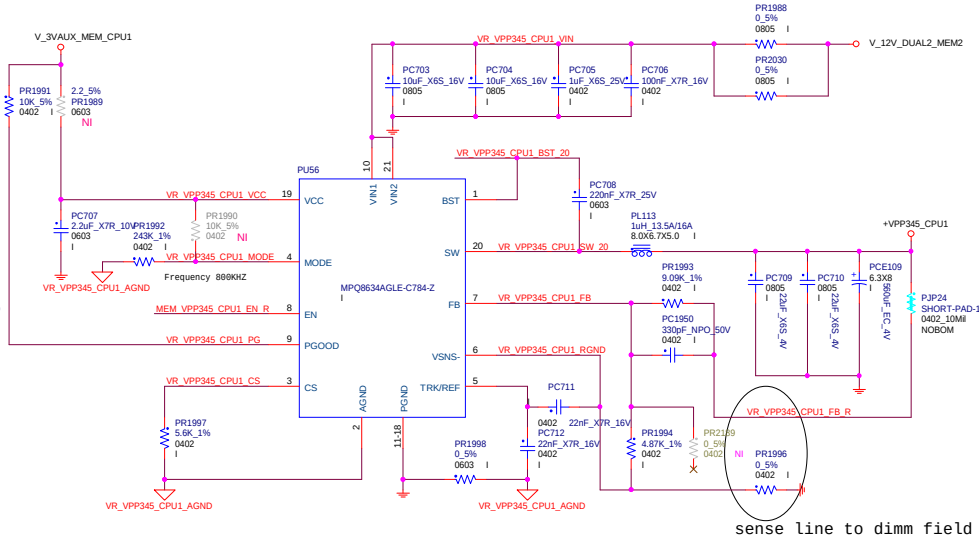
COMPRESSED IMAGE

CPU1 MEM VPP





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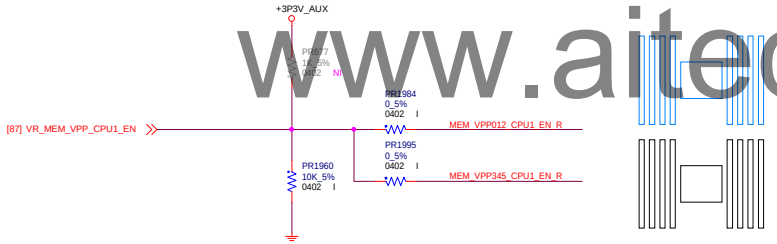

+2.575V / 6.77Atdc/8.922Apk

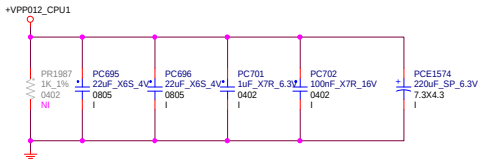

Table 227. PVPP_xxx VR Bulk / Decoupling Caps, per Neon City RB		
Cap Value	**Min Quantity per VR**	**Notes**
RB (25, Server) 6 DIMMs / VR		
560 µF / 4V / 10% / Alum THMT	1	Bulk, place close to VR output inductor
Cap Value	**Min Quantity per VR**	**Notes**
22.0 µF / 4V / 20% / X6S / 0805	6	Place 2 close to VR output inductor (bottom), 4 between DIMMs (top)
10.0 µF / 4V / 20% / X6S / 0603	8	Place between DIMMs, 2 caps/DIMM
Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.		

+2.575V / 6.77Atdc/8.922Apk

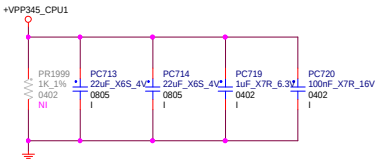

Table 227. PVPP_xxx VR Bulk / Decoupling Caps, per Neon City RB		
Cap Value	**Min Quantity per VR**	**Notes**
RB (25, Server) 6 DIMMs / VR		
560 µF / 4V / 10% / Alum THMT	1	Bulk, place close to VR output inductor
Cap Value	**Min Quantity per VR**	**Notes**
22.0 µF / 4V / 20% / X6S / 0805	6	Place 2 close to VR output inductor (bottom), 4 between DIMMs (top)
10.0 µF / 4V / 20% / X6S / 0603	8	Place between DIMMs, 2 caps/DIMM
Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.		

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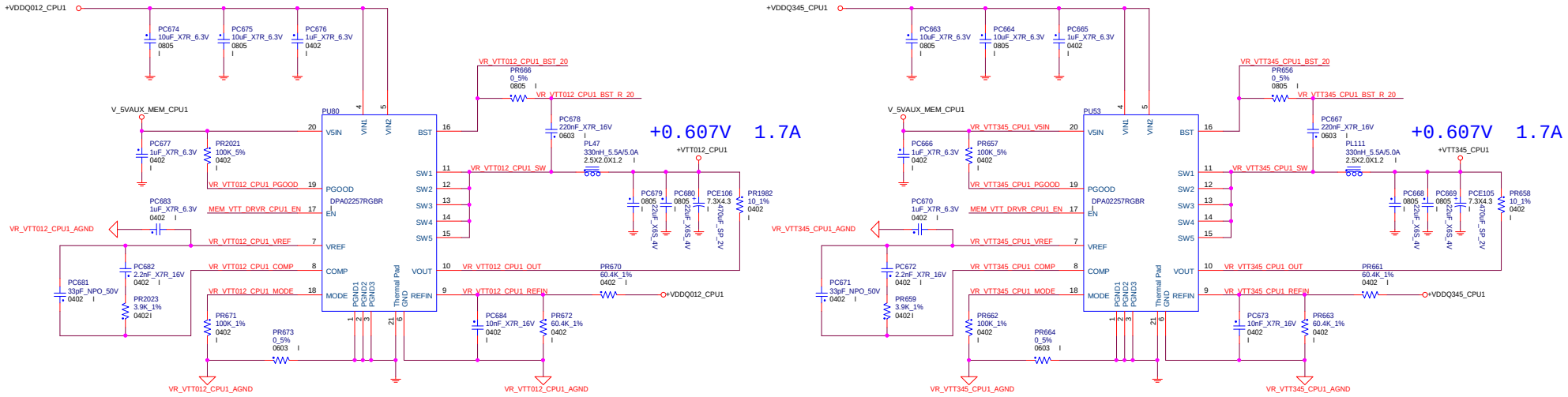
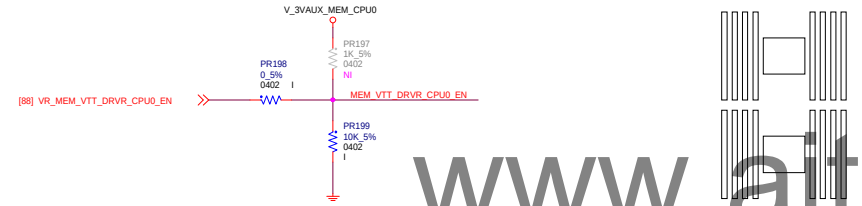
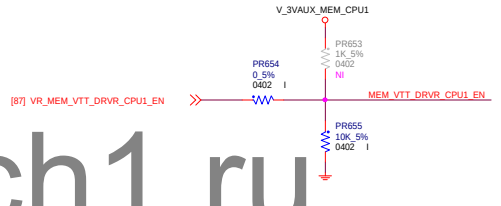
DDR_VTT







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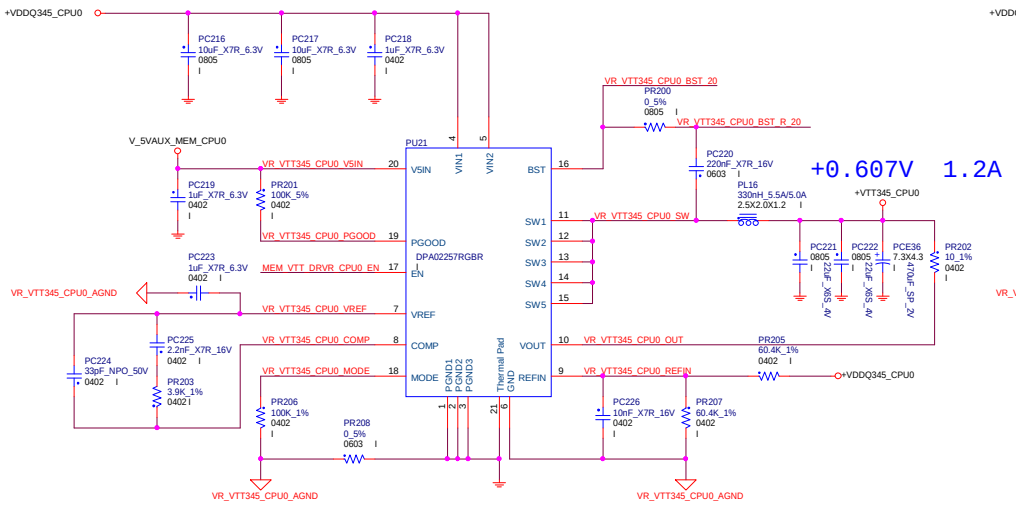

Table 225. PVTT_xxx VR (DDR4) Bulk/Decoupling Caps per RBs

Cap Value/ Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs / VR		
47 µF / 2.5V / 20% / X6S /0805	3	at VTT DIMM pin field
470 µF / 2.0V / 20% / Alum	1	Place close to VR output
22 µF /4.0V / 20% / X6S / 00805	1	
22 µF /4.0V / 20% / X5R / 0805	3	at VTT DIMM pin field

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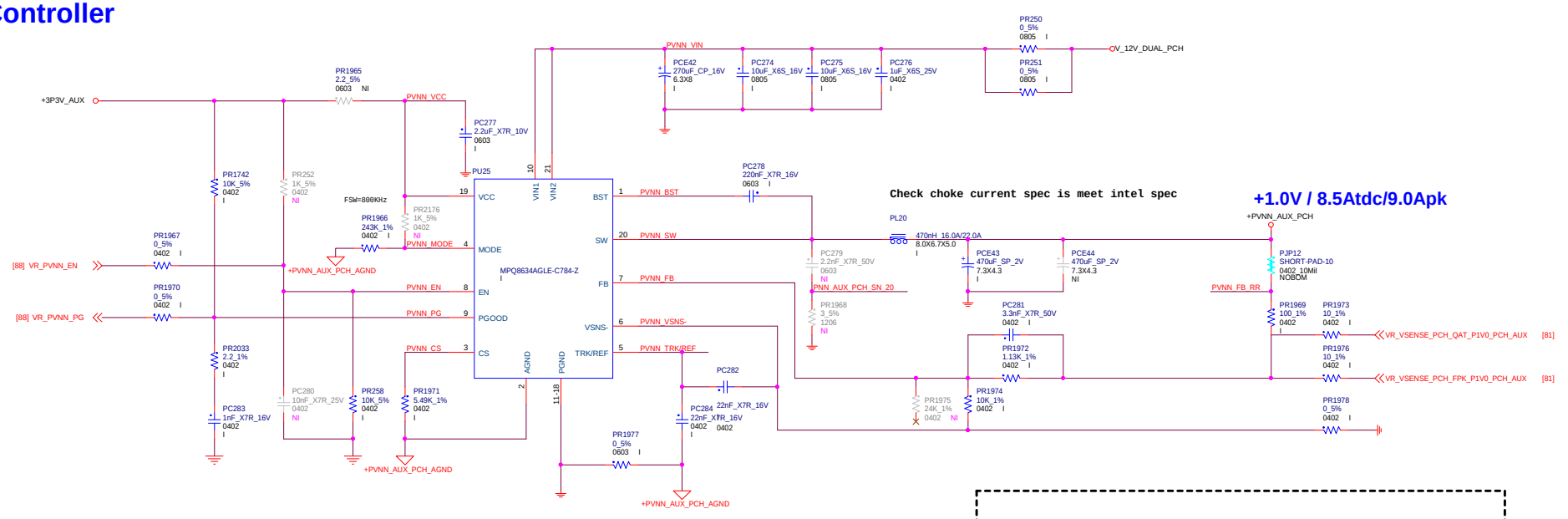
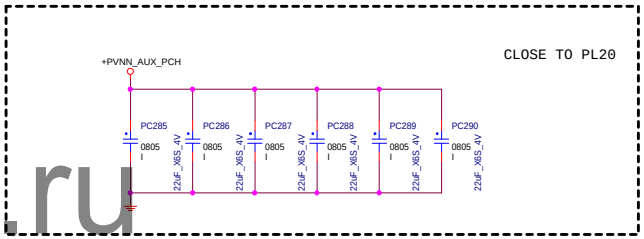
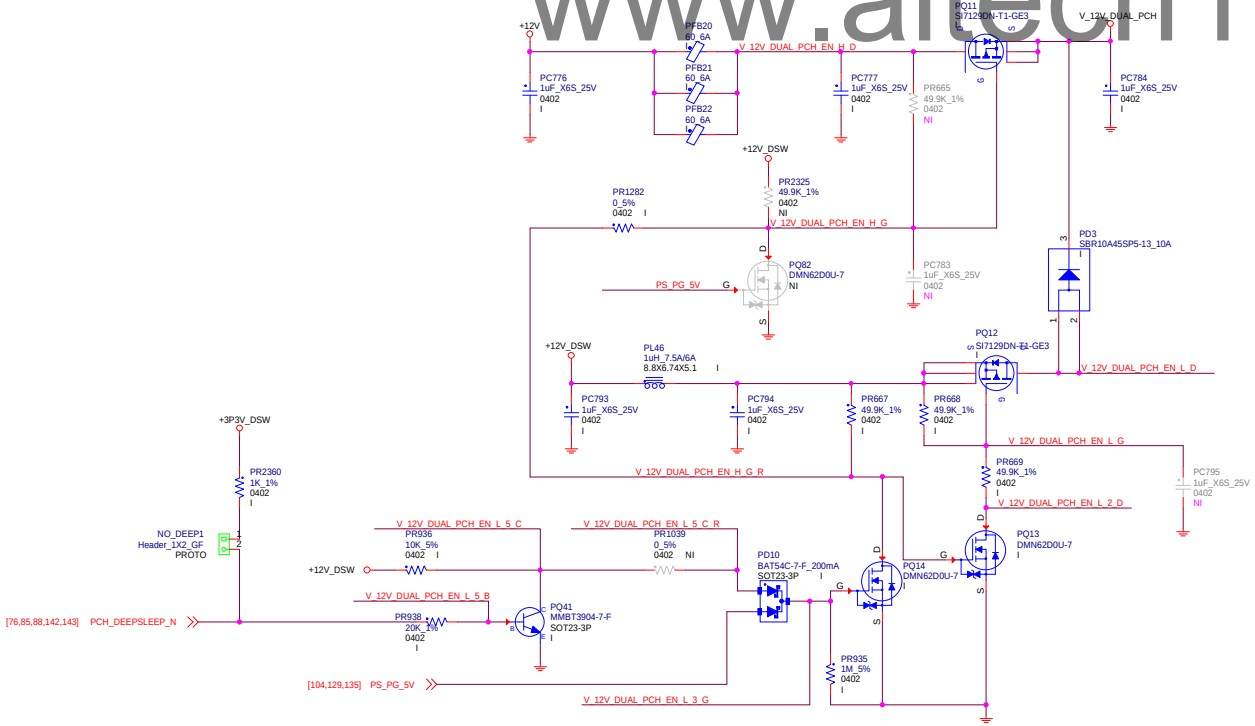
+VNN_Controller







PVNN_PCH_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 µF / 2.0V / 20% / AlPoly	3	bulk, place close to VR output inductor
47.0 µF / 4.0V / 20% / X6S / 0805	4	Place close to the PCH chip (bottom)
1.0 µF / 6.3V / 10% / X6S / 0402	18	Place close to the PCH
22.0 µF / 4.0V / 20% / X6S / 0603	18	Place close to the PCH (bottom)
22.0 µF / 4.0V / 20% / X6S / 0805	2	Place close to the VR Output Inductor (bottom)

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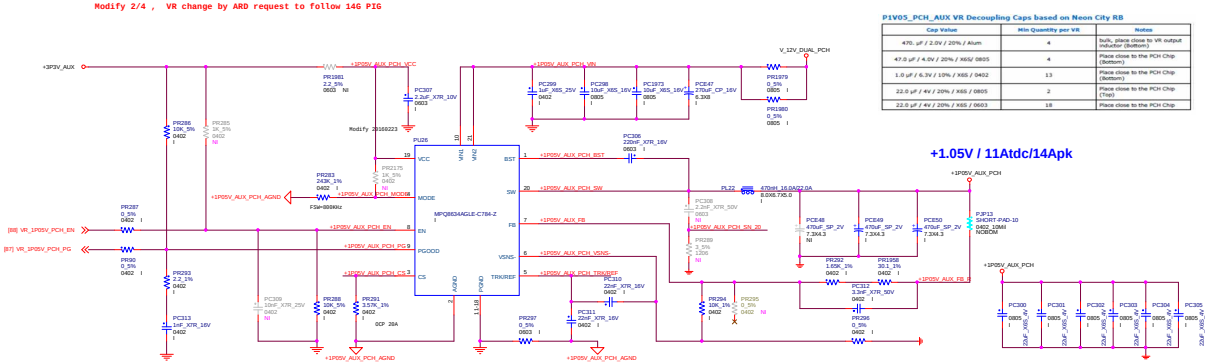
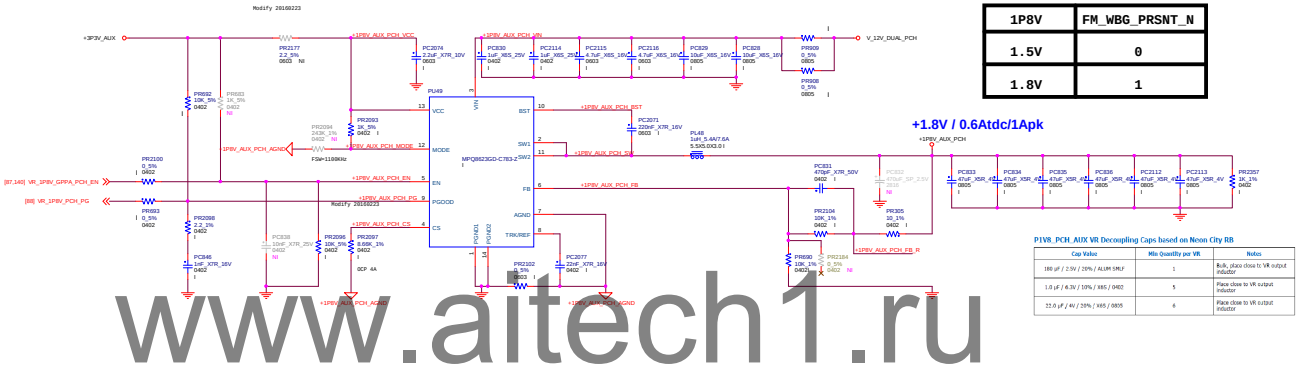
+1P05V_AUX_PCH_Controller



+1P8V_Controller



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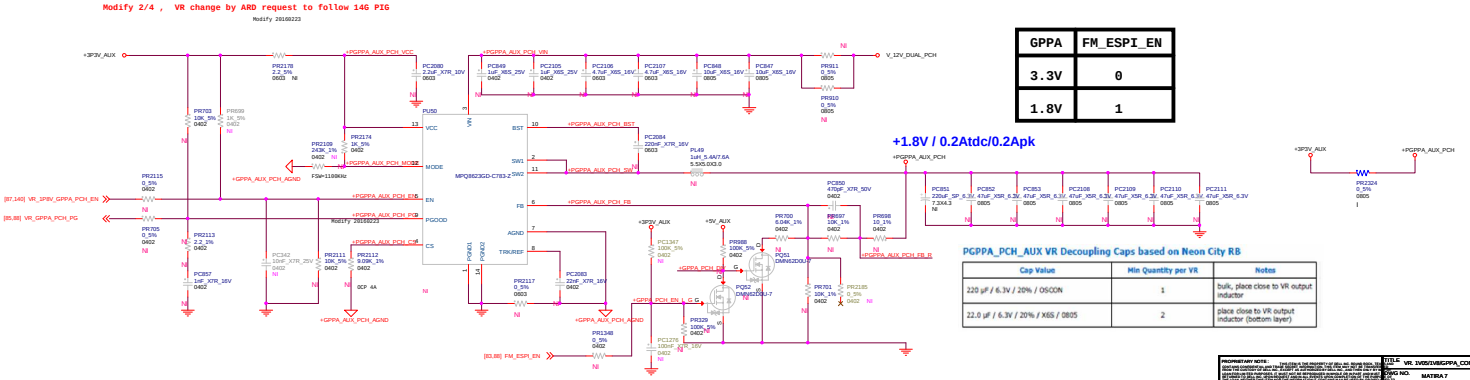
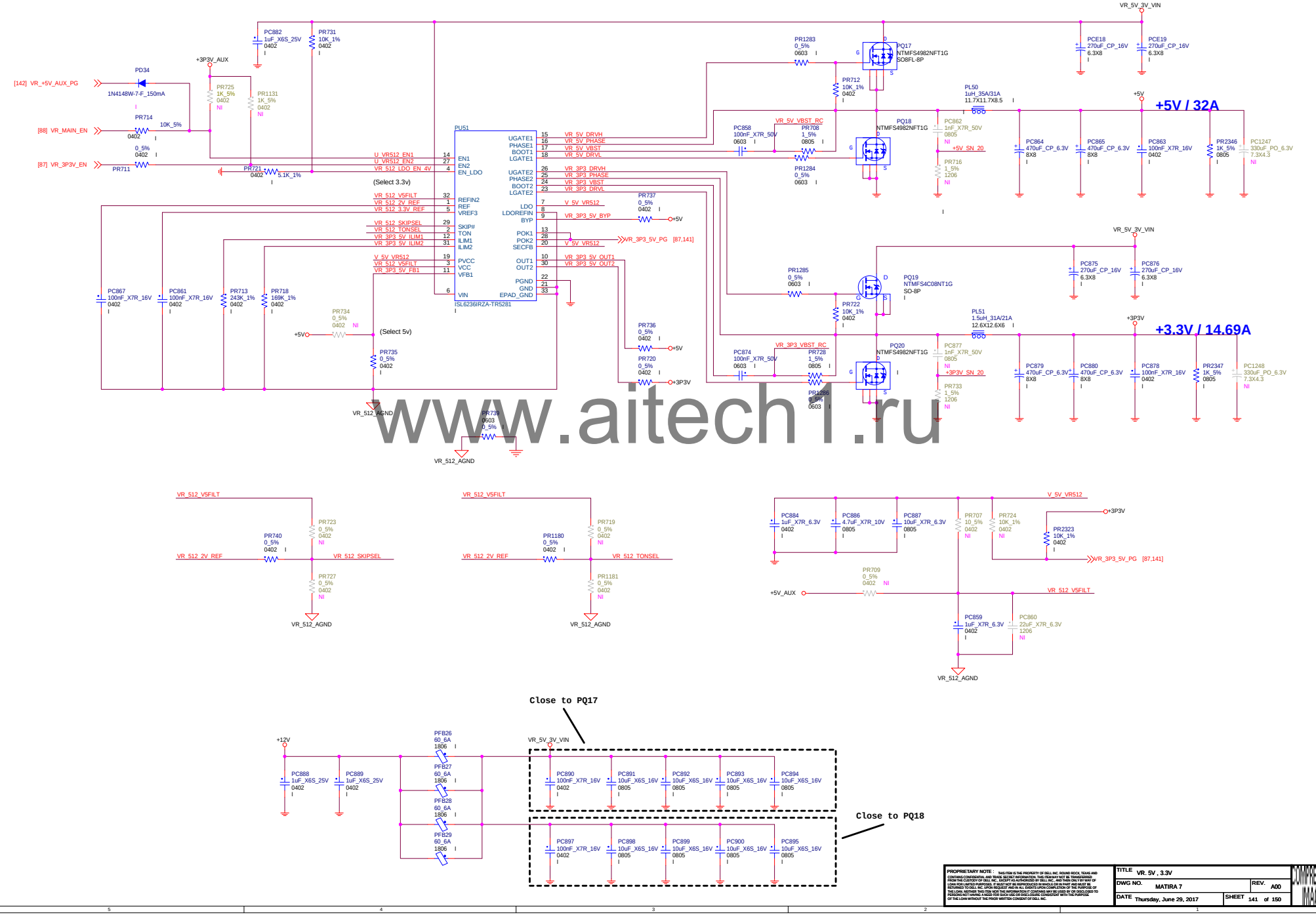
+PGPPA_Controller



+3V / +5V



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TITLE	VR. 5V , 3.3V
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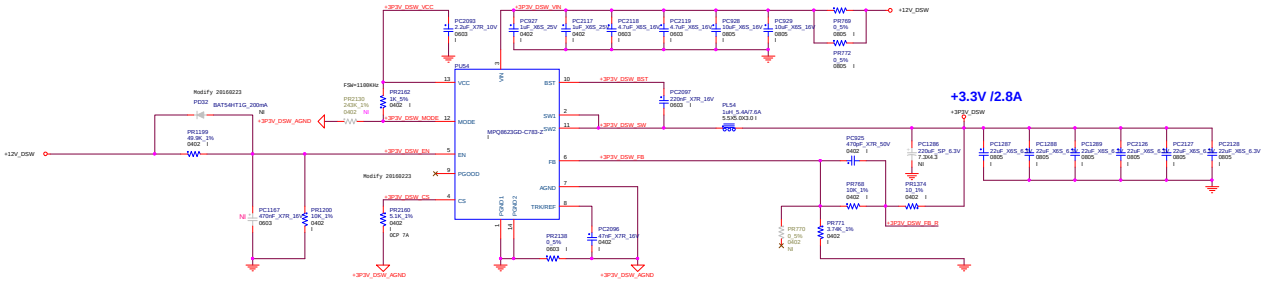
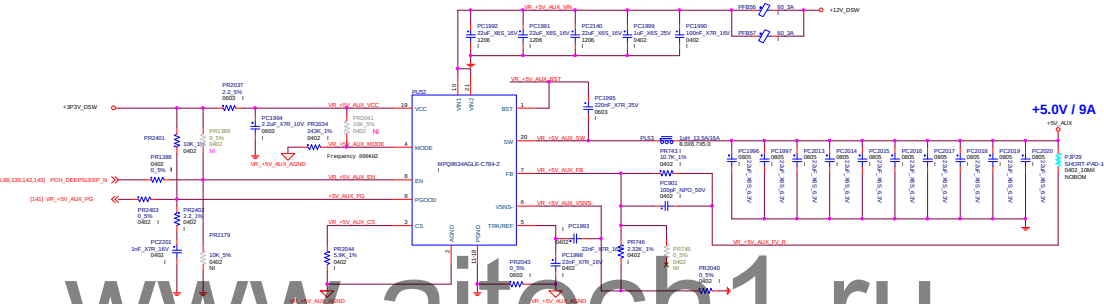
+3P3V_DSW

Modify 2/4 , VR change by ARD request to follow 14G PIG



+5V_AUX



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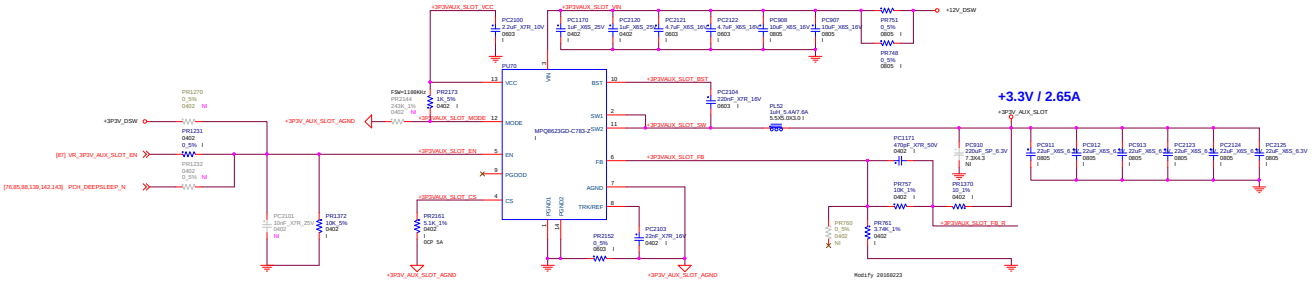
+3P3V_AUX_SLOT



TITLE	VR_+5V+3V_STDBY_CONTROLLER
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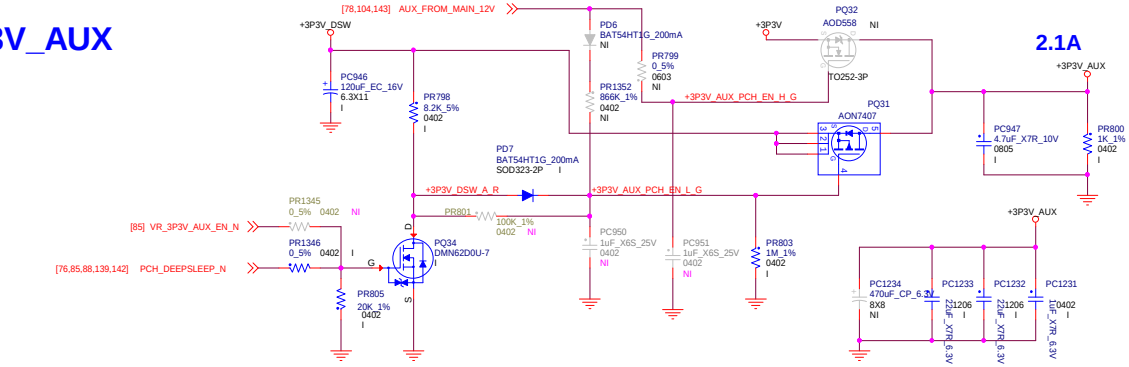
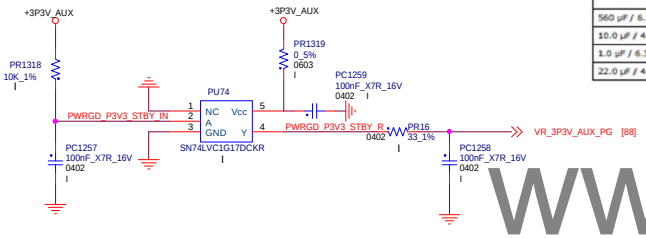
+3P3V_AUX

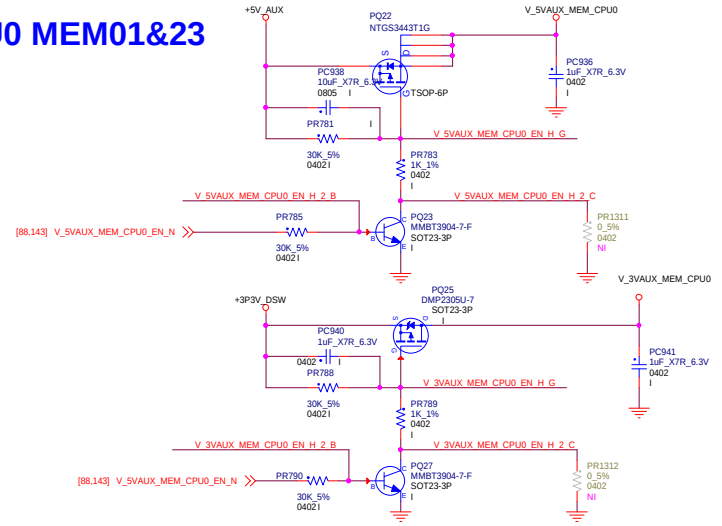


P3V3_AUX VR Decoupling Caps based on Neon City RB

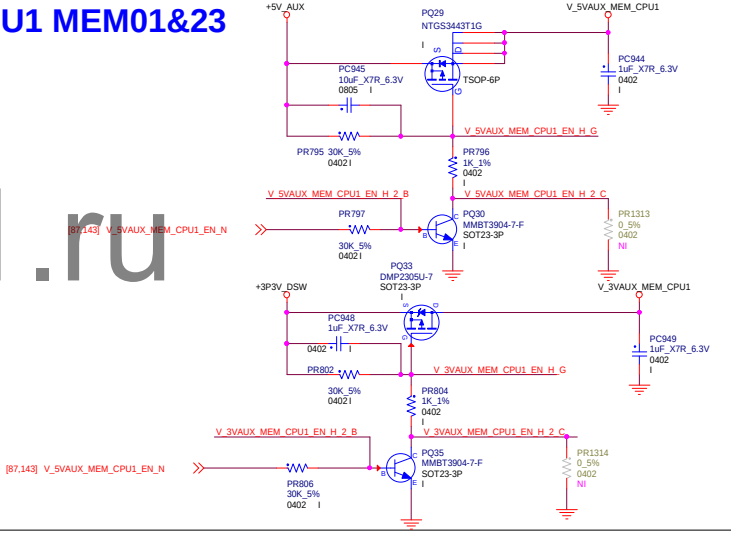
Cap Value	Min Quantity per VR	Notes
560 µF / 6.3V / 20% / Alum	1	Bulk, place close to VR output inductor
10.0 µF / 4.0V / 20% / X6S / 0603	6	
1.0 µF / 6.3V / 10% / X6S / 0402	3	
22.0 µF / 4.0V / 20% / X6S / 0805	2	Place close to VR output inductor



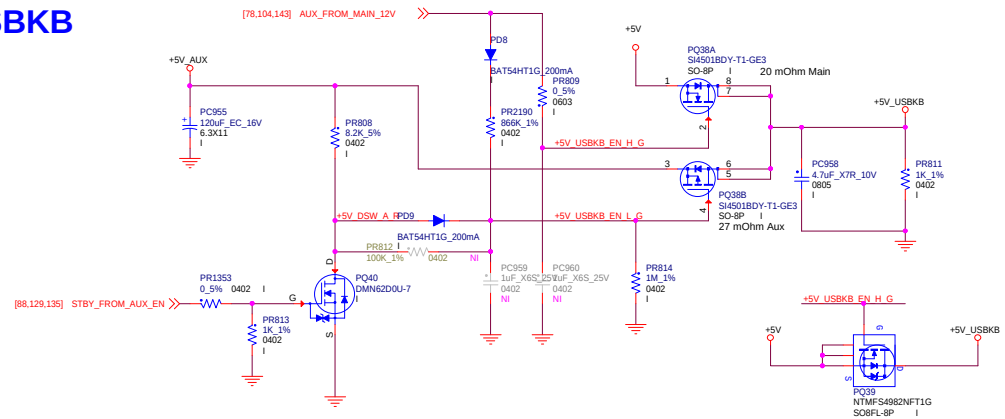
CPU0 MEM01&23



CPU1 MEM01&23



+5V_USBKB



+3V_EPW

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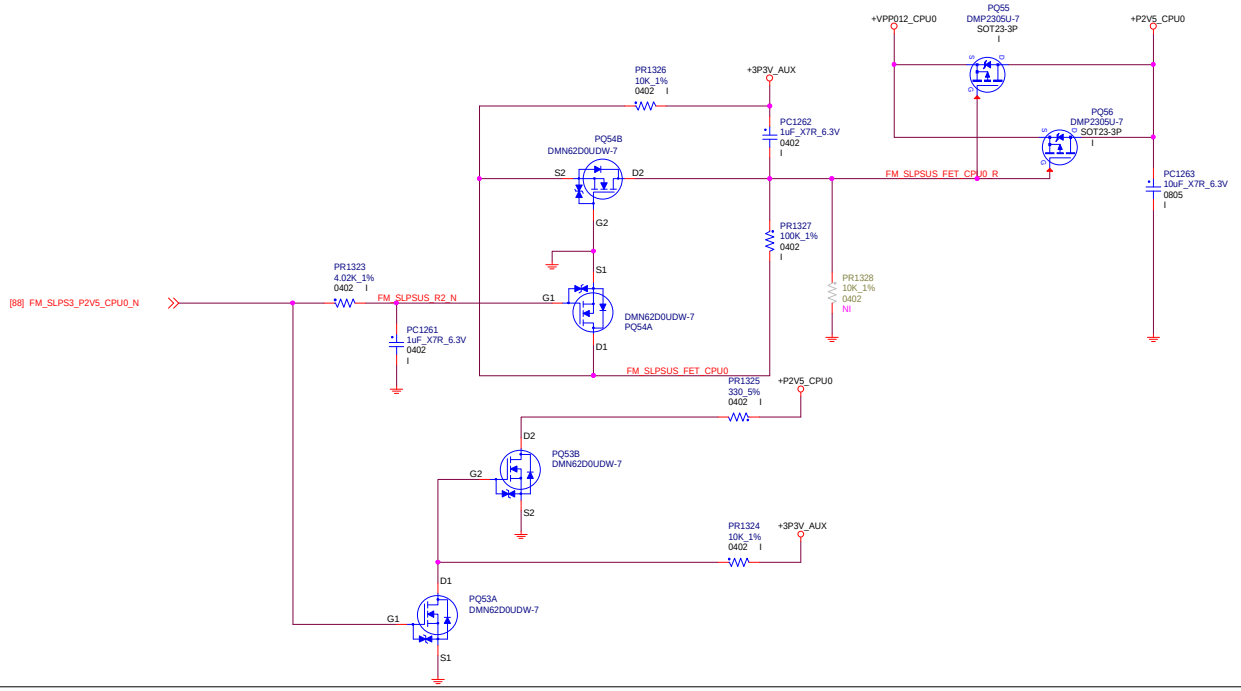
+P2V5_CPU0



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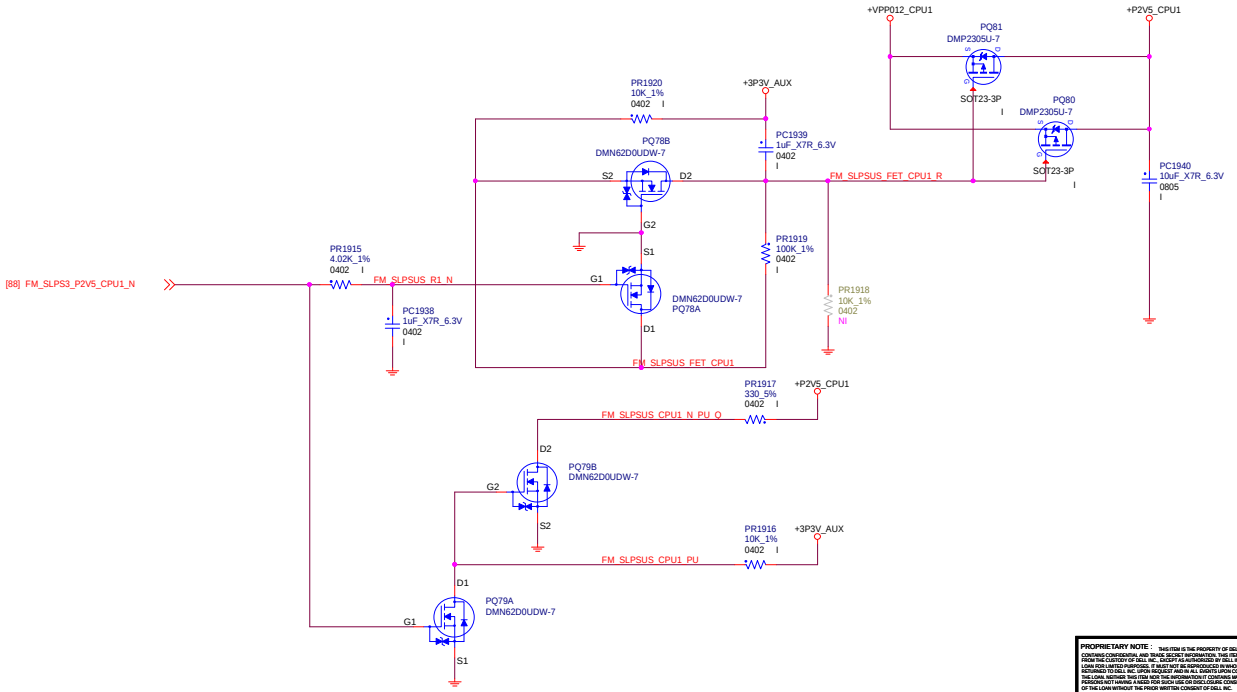
+P2V5_CPU1



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TITLE	LOADSWITCH, +P2V5_CPU0/1		
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TITLE	VR, USB3.1 VDD/VCC (EMPTY)		
DWG NO.	MATIRA 7	REV.	A00
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B00 to X00 changelist

20151005 EE

P088:DO3,RO195,RO201,RO205,RO206,RO209,CO84,CO85 change power net from +3P3V_AUX to +3P3V_CPLD

P104:Add RO311,RO310;but dummy RO310;Remove RP1,RP2;Dummy RP3,CP7;Modify QP3.G net from CPLD(UO1) A15 pin

P083:Modify RS135 and RS136 to 1K;Debug phase stuff RS135,Mass production stuff RS136

P085:Remove power sequence signals;Remove RO23,Add RO313,RO314;

P086:Remove power sequence signals;Remove RO181,RO182,RO166,RO167,RO176,RO177;

P109:Swap FM_CPU0_SKTOCC_LVT3_N and FM_CPU1_SKTOCC_LVT3_N at the series resistors RH374 and RH375;
Add RH381,QH11,QH12,XDP_DEBUG

P107:Add 32MByte flash and 2X5 pin header

P066:Add RC150

P067:Add RC151,RC152;but dummy RC152

P084:Modify XBT1 name to BATTERY name

20151005 DC

P113:PR44 connect to CPU0_VCCIN_VDD2,PR59 connect to CPU0_VCCIN_VDD3,PR60 connect to CPU0_VCCIN_VDD4,
PR75 connect to CPU0_VCCIN_VDD5,PR76 connect toCPU0_VCCIN_VDD6

P115:PR100 change from 100k ohm to 150k ohm

P121:PR205 connect to CPU0_VCCIN_VDD2,PR220 connect to CPU0_VCCIN_VDD3,PR221 connect to CPU0_VCCIN_VDD4,
PR236 connect to CPU0_VCCIN_VDD5,PR237 connect toCPU0_VCCIN_VDD6

P123:PR261 change from 100k ohm to 150k ohm

P129:PR367 connect to CPU0_VDDQ012_VDD2,PR381 connect to CPU0_VDDQ012_VDD3,Remove PC460¡BPC464,
R940 connect to +12V_DSW,PR941 connect to STBY_FROM_AUX_EN

P131:PR438 connect to CPU0_VDDQ345_VDD2,PR453 connect to CPU0_VDDQ345_VDD3.

P133:PR505 connect to CPU1_VDDQ012_VDD2,PR520 connect to CPU1_VDDQ012_VDD3.

P135:PR576 connect to CPU1_VDDQ345_VDD2,PR591 connect to CPU1_VDDQ345_VDD3,Remove PC650¡BPC609,
PR943 connect to +12V_DSW,PR944 connect to STBY_FROM_AUX_EN.

P137:Remove PC783¡BPC795,PR936 connect to +12V_DSW,Add 1x2 head PSW connect to PQ41.C & E.

P140:Change +3P3V_DSW solution to NCP3170,Change +5V_DSW solution to NCP3170,
Change +3P3V_AUX_SLOT solution to SN1309521RHL.

P141:Delete +3V_EPW control circuit.

20151008 EE

P094: Modify ECU3,ECU4 from DIP to SMD that SE request

P095: Modify ECU5,ECU6 from DIP to SMD that SE request

20151019 EE

P065: Modify RH216 power net to +VPP012_CPU0 from +VPP012_CPU1

20151023 EE

P067:Depop RC120 and pop RC119;Change net FM_PCIE_SCDB_PRSNT_0_N ~ FM_PCIE_SCDB_PRSNT_3_N location

P085,P088:Del CKBUF_EN net

P093:Change INT_SPKR material

P107:Modify SPI_DEBUG from 2X5 DIP to 2X4(1.27mm) SMD

20151015 DC

1.Memory Power IC PMbus pull high changed from V_3VAUX_MEM_CPU1 to +3P3V_AUX
2.unstuff : PR340¡BPR325¡BPR396¡BPR411¡BPR463¡BPR478¡BPR534¡BPR548 (for PMBUS pull high)

20151026 DC

P112¡GStuff PC1196
Change value by ti suggest¡G PR109 from 866k to 402k ¡BPR1295 from 14.7k to 56.2k¡B
PR102 from 150k to 20k¡BPR111 from 75k to 39k¡BR110 from 560k to 620k¡Aadd PR1387 4.02k
P113¡GStuff PR121
P123¡GStuff PC1198
Change value by ti suggest¡G PR270 from 866k to 402k ¡BPR1298 from 14.7k to 56.2k¡B
PR263 from 150k to 20k¡BPR272 from 75k to 39k¡BPR271 from 560k to 620k¡Aadd PR1385 4.02k
P124¡GStuff PR282
P131¡GStuff PR930 for GUI default setting
P133¡GStuff PR932 for GUI default setting
P137¡GUnstuff PR1210¡BStuff PR1212 for improve effeciency
P138¡GUnstuff PR1213¡BStuff PR1214 for improve effeciency

20151027 EE

P076 : RS202 change to 51K_1%

P109 : Add RH382,XDP_DEBUG1

20151027 DC

P104¡GChange POWER_BP_SIG for key pin different with audio connector.
Modify Power2 connector pin11 & 12 from +12V to +12V_DSW for layout routing.
P121¡GPCE6¡BPCE7¡BPCE8¡BPCE9 change size to £p6 for SE change air duck structure
P131¡GPCE10¡BPCE11¡BPCE25 change size to £p6 for SE chagne air duck structure

20151102 EE

P041 : Add CPU2_DIS connector,Add RH423,RH427,RH431;Dummy RH116,RH117

P064 : GTL2014 modify to BJT

P088 : FBO5 connect to +5V_AUX

P089 : RL205 connect to +5V_AUX

P092 : FBA4 connect to +5V_AUX

P093 : INT_SPKR change to 340687700-600-H same as D7

P104 : Power switch circuit move to FIO,modify FRONTPANEL pin7,8,9

P109 : Modify XDP_DEBUG --> XDP_CONSENT, XDP_DEBUG1 --> XDP_HALT

P101 : UU30,UU31,UU38,UU39 change to ESD7104MUTAG from ESD7004MUTAG

20151103 DC

P004¡GUpdate Power map
P104¡GRP3 connect to +5V_AUX¡ARP4 connect to +5V_AUX¡Adelete RO310,RO311
P138¡GPR988 connect to +5V_AUX.
P139¡GPR709 connect to +5V_AUX.
P140¡GPU52 enable pin connect to PCH_DEEPSLEEP_N.
P141¡GPQ29.S & PQ22.S & PQ38B.3 change power from +5V_DSW to +5V_AUX.
Delete +5V_DSW switch to +5V_AUX circuit.

20151119 EE

P063 : Change UPlink to PCIE Slot1
P068 : Change PCIE Slot1 from x4 to x8
P076 : Move 10G LAN from PCH 10G LAN to USB3/PCIE Port0
P097 : Change USB3.0 to USB2.0
P090 : Change LOM2 from X557 to I210

20151123 EE

P025 : Change CPU2_PC Sub-system from CPU0 to CPU1
P101 : Change USB3.1TypeC CONN to meet 1.6mm thick PCB
P105 : Change Thermal Sensor Circuit base on EC2016_HWM Proposal

20151125 EE

P075 : Modify SAS CONN signal basen on the late miniSAS CONN Pinout
P100 : Modify CC Switch from SLG to CCG4

20151202 EE

P068 : Modify SLOT1 from x16 to x8 CONN
P100 : Modify CCG4 circuit base on vendor's reply
P104 : Change miniSAS Front CONN to OCU_CONN

20151203 EE

P104 : Modify OCU_CONN pin define

20151210 DC

P124 :Modify PCE24 from 270uF/16V(dip) to 150uF/16V(SMD) by ME request.
P142-143 : delete LOM2 Power rail. (not support 10G)

20151210 DC

P112-114¡GChange VCCIN VR solution to infineon as Dell request.
P120-122¡GChange VCCIN VR solution to infineon as Dell request.
P128-135¡GChange VDDQ VR solution to infineon as Dell request.
P136-137¡GChange VPP VR solution to MPS as Dell request.
P138¡GChange VTT VR solution to Ti as Dell request.
P139-140¡GChange PCH VR solution to MPS as Dell request.
(VNN & 1.05VAUX)

20151217 EE

P078 : Add RS294,RS295

P087 : UO1 pin R5,P5 modify to MEM_VPP_CPU0_EN,MEM_VPP_CPU1_EN;
del RO221,RO222

20151221 EE

P075 : Add MINISAS CONN mounting screws
P102 : Add MINISAS CONN mounting screws
P104 : Update OCU_Front symbol link to cis

20151229 DC

P142¡GChange +5VAUX solution to MPQ8634A for USB charging in S5.
P145¡GFine tune USB3P1 VDD voltage to 1.22V ,
change PR1273 from 49.9k to 47k.

20151231 EE

P068 : Modify SLOT1_CPU1 Pin A1&A4&A11 to GND.
Modify objects CCL properties.

20160107 EE

P083 : Dummy RS141,ESPI_LPC_JUMPER

P084 : Modify TBT1 to 1X5 from 1X6

P088 : Add net FM_SLPS3_P2V5_CPU1_N to UO1 pin D16

P089 : Modify LAN1 library

P090 : Modify LAN2 library

P094 : Modify UU6 library

P095 : Modify UU1 library

P096 : Modify UU54 library

P097 : Modify UU27,UU49 library

P098 : Modify UU21 library

P099 : Add charing port

P101 : Modify UU33 library,change UU70,UU71 library
to DA1,DA2,DA3,DA4

P102 : Swap SATA port 6,7 RX

20160114 DC

P112¡B120¡B128¡B130¡B132¡B134¡G
Add 2 pair RC for Power Stage 2nd source
by Dell request.

20160115 EE

P107 : Modify TPM from NPCT650JAAYX_B to NPCT650JBAYX_B.

20160122 DC

Add VR HeatSink in Page 114¡B122¡B129¡B131¡B133¡B135

20160122 EE

P078 : Add USBPWR_6_F_EN

P095 : UU57 pin5 modify to +5V_AUX,UU1 pin5 modify to
USBPWR_6_F, UU18 pin1,13 modify to +3P3V_DSW

20160123 EE

1.Modify VDDQ decouple cap from 8*22uf to 9*44uf
Add CD379,CD388,CD396,CD405,CD413,CD420,CD427,CD434,
CD441,CD448,CD456,CD464,CD548,CD471,CD479,CD487,CD496,
CD505,CD513,CD520,CD527,CD533,CD540,CD547
P096 : Change Front USB3.0 CONN base on SE request

20160127 EE

P026 : Modify to meet Intel VRTT test spec.
CH102~CH146 from 10uF to 22uF,Del CH106;
CH22~CH61 from 22uF to 47uF,Del CH39;
Dummy RH379 for ES2 CPU can't boot issue
P027 : Modify to meet Intel VRTT test spec.
CH208~CH211 from 10uF to 22uF;
Add CH285~CH287
P048 : Modify to meet Intel VRTT test spec.
CH147~CH191 from 10uF to 22uF,Del CH165;
CH62~CH101 from 22uF to 47uF,Del CH88;
Dummy RH380 for ES2 CPU can't boot issue
P049 : Modify to meet Intel VRTT test spec.
CH212~CH215 from 10uF to 22uF;
Add CH288~CH290
P078 : Add GPO_SD_WP
P090 : Change UL3 vendor
P100 : Modify UU46 pin2,3 to +5V_AUX
P104 : Modify FRONTPANEL,OCU_FRONT pin define

20160129 DC

P113¡GChagne PStage driver pin resistor from 0402 to 0603 size.
P121¡GChagne PStage driver pin resistor from 0402 to 0603 size.
P129¡GChagne PStage driver pin resistor from 0402 to 0603 size.
P131¡GChagne PStage driver pin resistor from 0402 to 0603 size.
P133¡GChagne PStage driver pin resistor from 0402 to 0603 size.
P135¡GChagne PStage driver pin resistor from 0402 to 0603 size.

20160129 EE

P066 : Del CLK Buffer output port 5,6

P078 : Add CCG4_R_I2C_INT,CCG4_F_I2C_INT,MINISAS_HD_0_IFDET#,
MINISAS_HD_0_PRSNT#,MINISAS_HD_1_IFDET#,MINISAS_HD_1_PRSNT#

P087 : Del RO236 and net name RST_PCH_SCDB_PRSNT_N

P100 : Add UU65,UU66

P102 : Modify MINISAS_HD_0,MINISAS_HD_1 pin define

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TITLE	Changelist_A
DWG NO.	MATIRA 7
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UNCOMPRESSED IMAGE

B00 to X00 changelist

20160201 EE

P068,P069,P070,P071,P072,P073,P074 : Add FM_TBT_SCI_EVENT to B12 pin
P069,P070,P071,P072 : Add SLTx_CPUx_THROTTLE to B30 pin
P097 : Add SLT6_CPU1_THROTTLE,SLT7_CPU1_THROTTLE net name
P096 : Del ESD component

20160202 EE

P084 : Modify PCH_SKU component change to PROTO from NI
P085 : Modify I2C Bus and fan signal
P087 : del net name PUMP_TACH_CPU0,PUMP_TACH_CPU1
P105 : modify fan signal
P106 : modify fan signal
P110 : modify SMBus MUX

20160205 EE

P085 : Add SPI_2,SPI_SOCKET_2 peripheral component

20160215 DC

P129¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)
P131¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)
P133¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)
P135¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)

20160217 EE

P027¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)
P049¡GVDDQ MLCC change from 22uF to 47uF (Intel MOW update)
P105,P106¡GModify Fan signal follow ARD1.0

20160217 DC

P139¡GPop PR2033 & add PR2176 for other frequency option
P140¡GAdd PR2175 for other frequency option (1P05V_AUX)
add PR2177 pull high to Vcc pin , change PR2097 from 7.5k to 8.66k (1P8V_AUX)
add PR2178 pull high to Vcc pin , change PR2112 from 7.5k to 9.09k.(GPPA_AUX)
P142¡Gchange PR1199 from 30k to 49.9k , change PR771 from 3.57k to 3.74k (3P3V_DSW)
change PR2044 from 4.87k to 5.9k,add PR2179 pull down,change PR761 from 3.57k to 3.74k(3P3V_SLOTAUX) add 2 pcs 10uF/16V for +5VAUX
P145¡Gchange PR2172 from 7.5k to 6.65k ohm, change pc1161 from 470pF to 1nF.

20160218 EE

P066¡GAdd MIMISAS CLK
P084¡GModify TBT1 from 1X5 to 1X6
P102¡GModify MINISAS_HD_x signal
P110¡GModify fan MUX

20160222 EE by dell request

P029~P034: Del FM_ADR_COMPLETE_ABC_N
P035~P040: Del FM_ADR_COMPLETE_DEF_N
P051~P056: Del FM_ADR_COMPLETE_GHJ_N
P057~P062: Del FM_ADR_COMPLETE_KLM_N
P075,P078: Modify MINISAS_HD_2~MINISAS_HD_5 pin definition

P076¡GModify US6 to APX809-29SAG-7 from ADM1085AKSZ-REEL7
US4 pin3 modfiy to +3P3V_AUX from +3P3V_DSW

P079¡GDelete QS4,RS56,RS57,RS58,RS59,RS60,RS61,RS62
P086¡GDummy UQ06,UQ7, QQ23, QQ24, RQ179, RQ180
P087¡GDel EC_CPLD_ENABLE,RQ155
P088¡GDel UQ1 pin B16 about ADR_COMPLETE_DLY

20160224 EE

P065¡Gcombine all_DIMM_EVENT_N signals together into one MEMHOT_N signal
P068~P074¡GAdd net name SLOTx_B12_EVENT
P078¡GAdd net name HDD_TEMP_DET1~4#,GPI_TBT_CABLE_N
P084¡GAdd net name GPI_TBT_CABLE_N
P085¡GAdd net name SLOTx_B12_EVENT,EC_B12_EVENT_SM_MEM_EVENT_N
P088¡GDel net name SM_MEM_EVENT_RIGHT_N,SM_MEM_EVENT_LEFT_N
P104¡GModify POWER_BP_SIG for HDD_TEMP_DET1~4#

20160224 DC

P112¡GCombine VRHOT & MP2 pull high to +3P3VAUX into one signal : VR_HOT_N
delete signal VR_CPU0_VCCIN_PIN_ALT_N
depopulate PR33
P112¡GCombine VRHOT & MP2 pull high to +3P3VAUX into one signal : VR_HOT_N
delete signal VR_CPU1_VCCIN_PIN_ALT_N
depopulate PR485
P128¡GCombine VRHOT & MP2 pull high to +3P3VAUX into one signal : VR_HOT_N
add PR2180 for debug
depopulate PR2001
P129¡GChange PR160 from 1k to 120 ohm to meet Intel power sequence
P130¡GCombine VR_HOT & MP2 pull high to +3P3VAUX into one signal : VRHOT_N
add PR2181 for debug
depopulate PR2004
P131¡GChange PR195 from 1k to 120 ohm to meet Intel power sequence
P132¡GCombine VR_HOT & MP2 pull high to +3P3VAUX into one signal : VRHOT_N
add PR2182 for debug
depopulate PR2007
P133¡GChange PR616 from 1k to 120 ohm to meet Intel power sequence
P134¡GCombine VRHOT & MP2 pull high to +3P3VAUX into one signal : VR_HOT_N
add PR2183 for debug
depopulate PR2010
P135¡GChange PR651 from 1k to 120 ohm to meet Intel power sequence

20160225 EE

P075¡GModify MINISAS_HD_2~5 pin define
P078¡GAdd HDx_GPIO1 signal
P084¡GModify TBT1 to 1X5

20160301 EE

P078,P079 : Modify SLOTx_B12_EVENT signal

P079,P088 : Delete FM_ADR_SMI_GPIO_N

P085 : Add VR_HOT_N,remove VR_MEM012_CPUx_VRHOT_N,
VR_MEM345_CPUx_VRHOT_N,add SMSC request

20160301 DC

P114¡GChange PR75 from 5.49k to 4.7k
Change PR2065 from 5.49k to 0
Change PR2015 from 931 to 5.36k
pop PR72; depop PR73
P115¡GChange PR101 from 9.31k to 8.25k
Change PR109 from 402k to 412k,Delete PR1295
Change PR113 69.8k from to 71.5k,Delete PR1301
Chagne PRT1 from 100k to 10k & depop
Change PR110 from 620k to 487k
Change PR100 from 150k to 39k;Delete PR1385
Change PR108 from 75k to 100k
Change PR105 from 2.61k to 2.67k
Change PC127 from 330nF to 470nF
Change PC126 from 1.5n to 2.2nF
Change PR106 from 5.76k to 12.4k;Depop PC125
P116¡GChange PL58 from 0.24uH to 0.47uH
Change PR120 from 13.7k to 3.3k
Change PR121 from 100k to 33k
Change PRT2 from 100k to 10k
Change PC1241 from 6.8n to 100nF
Change PR1023 from 22.6k to 4.99k;Delete PC142
P122¡GChange PR530 from 5.49k to 4.7k
Change PR2067 from 5.49k to 0
Change PR2012 from 931 to 5.36k
pop PR527; depop PR528
P123¡GChange PR262 from 9.31k to 8.25k
Change PR270 from 402k to 412k;Delete PR1298
Change PR274 69.8k from to 71.5k; Delete PR1303
Chagne PRT5 from 100k to 10k & depop
Change PR271 from 620k to 487k
Change PR261 from 150k to 39k;Delete PR1387
Change PR269 from 75k to 100k
Change PR266 from 2.61k to 2.67k
Change PC325 from 330nF to 470nF
Change PC324 from 1.5n to 2.2nF
Change PR267 from 5.76k to 12.4k
Depop PC323 , PR264
P124¡GChange PL57 from 0.24uH to 0.47uH
Change PR281 from 13.7k to 3.3k
Change PR282 from 100k to 33k
Change PRT6 from 100k to 10k
Change PC340 from 6.8n to 100nF
Change PR1024 from 22.6k to 4.99k
Delete PC1242

20160302 EE

P085,P087,P104¡GDel GPO_AMBER_N and GPO_WHITE_N from EC
and change name to PWRLED_AMBER_N and PWRLED_WHITE_N

P087¡GAdd FLASH_EN# signal
P096¡GModify ECU10,ECU12 package
P100¡GModify UU65,UU66
P104¡GModify POWER_BP_SIG library
P106¡GModify UQ16 library
P107¡GModify ROM_DIS,Add FLASH_EN# signal

20160304 EE

P085¡GAdd RQ419~RQ422

P087,P136,P137¡GRename MEM_VPP_CPU0_EN/MEM_VPP_CPU1_EN to
VR_MEM_VPP_CPU0_EN/VR_MEM_VPP_CPU1_EN

P041,P088¡GAdd net name H_CPU1_PROCDIS_COD_GTL_N to CPLD
P089¡GModify RL13 power net to +3P3V_DSW for auto power on issue
P103¡GModify UO8 IC

20160308 EE

P080¡GModify LS1
P082¡GModify PCH_HEATSINK
P085¡GDel FM_ESPI_EN signal,Del RO33
P086¡GDel UQ6,UQ7,QQ23,QQ24
P088¡GDel VR_CPU0_VCCIN_VR_HOT_N,VR_CPU1_VCCIN_VR_HOT_N signal

20160308 DC

P112¡GChange PR4 from 1k to 10k

P120¡GChange PR456 from 1k to 10k

P128¡GChange PR131 from 1k to 10k

P130¡GChange PR172 from 1k to 10k

P132¡GChange PR587 from 1k to 10k

P134¡GChange PR628 from 1k to 10k

P136¡GAdd PR2186¡BPR2187 (depop) for RSV team test

P137¡GAdd PR2188¡BPR2189 (depop) for RSV team test

P138¡GChange PL47 from 240nH to 330nH
Change PL111 from 240nH to 330nH
Change PL16 from 240nH to 330nH
Change PL17 from 240nH to 330nH
Change PU21¡BPU22 V5IN pin from 5VAUX to V_5VAUX_MEM_CPU1
Change PU80¡BPU53 V5IN pin from 5VAUX to V_5VAUX_MEM_CPU0

P139¡GChange PU25 from MPQ8634B to MPQ8634A
Change PR1971 from 5.76k to 5.49k

P140¡GChange PU26 from MPQ8634B to MPQ8634A
Change PR291 from 6.81k to 3.57k
Rename GPPA AGND
Depop PC832
Add PR2184¡BPR2185 (depop) for RSV team test

P140¡GDepop PC950¡BPC951¡BPC959¡BPC960

20160311 EE

P076~P082¡GUpdate PCH symbol
P079,P087,P088¡GAdd disable LOM1,LOM2,USB3.1
(front and rear) ,TPM,SD signal

P085,P088¡GAdd EC_RSMRST_N
P085¡GModify EC_JTAG library
P104¡GDel RO141

20160315 EE

P064¡Gdel FM_CPU0_EAR_G_N,FM_CPU1_EAR_G_N,FM_CPU_EAR_LVT_N peripheral component
P079¡GAdd RS299,RS300,RS301,RS302,RS303,RS304,RS305,RS306
P085¡GAdd RQ429,RQ431,RQ432,remove RQ334;modify EC_JTAG_RST;
P087¡GAdd RO430;del RO223,RO224,PCH_SUSWARN_N,PCH_SUSACK_N,FM_CPU_EAR_LVT_N
P101¡GModify UU30,UU31,UU38,UU39 library

20160316 EE

P068~P072¡GModify slot part reference to SLOTx_CPUx

P078¡GDel FM_PLD_PCH_DATA,RS223,FM_PS_PWROK_DLY_SEL,RS257,PCH_CPUPCIE_RST_GPPB19,RS263

P085¡GDel FM_SLP_SUS_RSM_RST_N

P087¡GDel FM_PLD_PCH_DATA,FM_PS_PWROK_DLY_SEL

P088¡GDel RO208,RO209,FM_JTAG_EN_DEBUG,FM_PCH_PRSNT_N,FM_SLP_SUS_RSM_RST_N,QO25,RO210,
RO211,FM_WBG_PRSNT_N,RO158,PCH_CPUPCIE_RST_GPPB19

20160316 DC

P138¡GChange VTT ouput cap from 470uF/2.5V to 470uF/2V (Dell assign PN)
P139¡GNO_DEEP header BOM change to PROTO
P140¡GChange GPPA output cap voltage rate from 4V to 6.3V
Delete PR1350¡BPR1351¡BPQ15¡BPR689¡BPC2085
Change PR690 from 15k to 10k.

20160317 EE

P083¡GStuff RS141 for LPC bus;modify PU_CPLD_LPC_ESPI_STRAP net name to FM_ESPI_EN
P085¡GModify EC VIN net name to EC1_VR_CAP;modify RO387 to 10K;modiyf SPI_2 to 4M-bit;
add EC_SPI_DEBUG;add PS_LOAD,PS_STAT1,PS_STAT2

P087¡GDel PCH_PWRBTN_N(PL3D/G6 pin)
P088¡GDel RST_LPC_ESPI_LEGACY_N,RQ234,PU_CPLD_LPC_ESPI_STRAP,PS_LOAD,PS_STAT1,PS_STAT2
P100¡GModify RF251,RF254 to 680 ohm
P106¡GModify UO14 to EMC2303-1-KP-TR_B
P108¡GModify LPC_ESPI_DEBUG peripheral component

20160318 EE

P084¡GAdd SATA_RAID_KEY
P085¡GModify EC JTAG signal
P088¡GModify CPLD I2C Bus net name to I2C_FRONT_FAN_SCL(SDA)
P110¡GModify UO13 peripheral component

20160321 EE

P029~P040¡GModify DIMM part reference to DIMMx_CPU0
P051~P062¡GModify DIMM part reference to DIMMx_CPU1
P092¡GAdd CA114~CA116;Modify RA31~RA33 to short pin
P106¡GModify RO112 power net to +3P3V

20160322 EE

P003¡GModify SMBus block diagram
P079: SATAGPx and SSATAGPx signal as 10k pull-down
P085¡GAdd RO439,RO440
P093¡GAdd FBA12,FBA13
P100¡GAdd RU536,RU537
P105¡GModify FAN_CPU0,FAN_CEN_CPU control signal
P107¡GAdd SPI_3
P110¡GModify UO10,UO11,UO13 and peripheral component

20160323 EE

P079¡GAdd PCH_LAN_DIS_N,PCH_PCI_DIS_N PD to 10K ohm
P085¡GChange EC_JTAG CONN from DIP to SMD,RO387 change to 4.7K ohm

20160324 DC

P138: Change PR671,PR662,PR215,,PR205 from 68K to 100K,Change TPS53317 to DPA02257RGBR
P143: Add PR2190,change PR1352=866k.

20160324 EE

P068~P074,P078¡GAdd pull high 10k ohm to SLOTx_B12_EVENT and depopulate pull down resister
P078¡GAdd RS363
P079¡GAdd RS364
P084¡GModify SATA_RAID_KEY library
P085¡GDel CO128;add RO441,RO444;for LPC Bus stuff RO429,RO431,RO307,RO45,dummy RO124;
for boot non-shared SPI bus :stuff RO384,RO414,dummy RO415,RO413;add CPUx_PUMP_DET#

P101¡GModify UU30,UU31,UU38,UU39 library
P105¡GModify fan connector to 7 pin

20160325 EE

P025¡GModify CPUx_P0_A,CPUx_P0_B library
P084¡GUpdate TBT1 library

20160325 DC

P129: change PC155 from 1uf MLCC to 6.3X8 16V OS-CON CAP

20160328 EE

P084: Add PASSWORD_CMOS_CLR_SERVICE_MODE,del Password_CLR,CMOS_CLR,SERVICE_MODE
P101: Modify USB31_TC_REAR_A,USB31_TC_REAR_B P1,P2 pin

20160329 EE

P069~P072: Modify SLOTx_CPUx_LATCH1 part reference
P085: Add GPIO204
P107: Modify CF9,CF10 to 1uF

20160330 EE

P085: Add SLTx_CPUx_THROTTLE_CPLD_EC_I2C_ALERT#
P087: Del SLTx_CPUx_THROTTLE;modify UO1 library
P088: Del SLTx_CPUx_THROTTLE;add CPLD_EC_I2C_ALERT#,RO445;modify UO1 library
P092: Modify FBA5 library
P105: Modify FAN_CEN_CPU1,FAN_CPU0 library

20160331 EE

P019: Stuff RH30;dummy RH48;enable TXT function
P041: Dummy RH124;enable TXT function
P108: Modify LBL1 library

20160406 EE

P066: Stuff RC156;dummy RC155;add RC157,CC27,CPLD_CKBUF_EN
P078: Del RS297
P087: Add CPLD_CKBUF_EN
P088: Modify RO159 to 49.9 ohm
P109: Modify RH273,RH274,RH275,RH276 to 100 ohm

20160407 EE

P085: Add test point TP91,TP92
P087: Add test point TP89,TP90
P111: Modify MH1~MH12 library

20160408 EE

P066: Modify UC1,UF3 library
P085: Dummy RO126;Modify UO_EC to MEC5105K-TMP2-TN
P100: Modify UU64 to temp. foxconn p/n

20160411 EE

P068: Modify SLOT1 CPU0 library
P100: Stuff UU65,UU66,RU562,RU563;Dummy RU536,
RU537
P105: Modify FAN_CPU0,FAN_CEN_CPU1 library

20160415 EE

P079: Dummy RS227,RS228

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X00 to X01 modify list

20160426 EE

P066 : Del UF3 and peripheral component
P078 : Modify HD5_GPIO1,GPI_TBT_CABLE_N to HDD_TEMP_DET3#,HDD_TEMP_DET4# location
P079 : Add FM_PCIE_SCDB_PRSNT_0~3_N,GPI_INTRUDER_CABLE_DET_N
P084 : AUX_LED,RS130,TBT1,RS86,RS87,RS88 change to PROTO
P085 : add 2 pcs 0 ohm to VTR3(NS) for +PGPPA_AUX_PCH and V_3P3_AUX_EC
P085 : add 2 pcs 0 ohm to VTR3(NS) for +PGPPA_AUX_PCH and V_3P3_AUX_EC
P087 : Del GPI_INTRUDER_CABLE_DET_N
P088 : Add USB3.0 re-driver
P099,100,101 : Del USB3.1 and peripheral component
P099 : Add USB3.0 connector and peripheral component
P103 : Modify UO8 and peripheral component
P104 : Del OCU_FRONT and peripheral component,modify FRONTPANEL,POWER_BP_SIG pin definite
P109 : CH18 link to +1P05V_AUX_PCH
P110 : Del UO13 and peripheral component
P145 : Del USB3.1 power

20160428 EE

P079 : Add RS365,RS366
P088 : Modify RO243,RO244 net name to I2C_PCIE_MUX_xxx
P094 : Modify RU35.2 net name change to PCH_USB_OC2_N;dummy RU35
P096 : Del UU58,UU59 and peripheral component;modify USB3_FRONT1 pin1,19 power net.
P097 : Add RU666 and modify net to PCH_USB_OC6_N
P098 : Del UU62,UU63 and peripheral component;Modify USB3_INT1 pin1,19 power net;
modify UU21 pin 5 power net.
P108 : Modify LBL1 library

20160504 EE

Lewisburg SE IO Power On Customer feedback issue

P069 : Add RX122
P069 : Add RX121
P070 : Add RX119
P071 : Add RX117
P072 : Add RX116
P073 : Add RX120
P074 : Add RX118
P075 : Add RX112~RX115;modify RX64~RX67 to 200 ohm.
P084 : Add RS367,RS368,RS370
P093 : Add RA65;modify RA12 to 200 ohm
P096 : Add RU668
P096 : Add RU669
P098 : Add RU667
P102 : Modify RT37~RT40 to 200 ohm
P104 : Add RP11~RP13

20160505 EE

P077 : Add ODD_SATA signal
P079 : Add RS369,del PCH_FUSB31_DISABLE_N,PCH_RUSB31_DISABLE_N,
PCH_SD_DISABLE_N,RS393,RS394,RS395
P087 : Del PCH_FUSB31_DISABLE_N,PCH_RUSB31_DISABLE_N
P088 : Del PCH_SD_DISABLE_N
P102 : Add ODD_SATA

20160506 DC

P115 : Add PR2195
P123 : Add PR2196
P128 : Add PR2191
P130 : Add PR2192
P132 : Add PR2193
P134 : Add PR2194
P136 : Change PCE38¡BPCE40 package to short cut
P137 : Change PCE107¡BPCE109 package to short cut
P141 : Change PC875¡BPC876 to Dell PIC part

20160509 EE

P066 : Modify Clock buffer
P067 : Modify Clock buffer
P079 : Add RS371
P087 : Del net name CLK_CPU1_BCLKS_EN_N

20160516 EE

P066 : Update FBC2 from MMZ2012S601A to MMZ2012S601AT
P067 : Update FBC4 from MMZ2012S601A to MMZ2012S601AT
P075 : Update MiniSAS CONN Screw PN
P080 : Update LS1 from MLH2012F22NKT to MLH2012F22NKT000
P085 : Modify EC_SPI_DEBUG pin define,update SPI_2 to large package;
fix BITS284787
P102 : Update MiniSAS CONN Screw PN
P104 : Modify POWER_BP_SIG&FRONTPANEL CONN PN
P107 : Modify SPI_DEBUG pin define;fix BITS284787
P111 : Update PCB Supplier PN and mouting hole footprint

20160517 EE

P066 : Update UC3 PN and footprint
P067 : Update UC2 PN and footprint
P085 : Modify SPI_2 package from SMD to DIP
P098 : Remove Redriver for FIO USB DCI function
P104 : Update Frontpanel footprint

20160517_1530 EE

P064,P065 : Update Common logic base on DELL EE tracker item56

P064,P065:Must check it.

20160519 EE

P066 : Add LOM1 clock
P076 : Del LOM1 clock
P083 : Dummy ESPI_LPC_JUMPER
P104 : Modify POWER_BP_SIG connector to 2X9
P107 : Dummy ROM_DIS(2-3)

20160519 EE

P025 : Update CPU_BP from W/ NUT to W/O NUT
P079 : Add FVS and UEFI test point
P104 : Modify Frontpanel from R/A to vertical

20160520 EE

P111 : Modify PCB main source from Tripod to BTI

20160520 DC

Change IFX PN to new one (include firmware)
Q1120,Q1121,Q1122,Q1123,Q1124,Q1125,Q1126,Q1127,Q1128,Q1129,Q1130,Q1131,Q1132,Q1133,Q1134,Q1135,Q1136,Q1137,Q1138,Q1139,Q1140,Q1141,Q1142:Change Material from 32023VE00-221-G to 320240D00-221-G
P120:Change PU53 PN from 32023VE00-221-G to 320240D00-221-G
P128:Change PU12 PN from 32023VP00-221-G to320240F00-221-G
P130:Change PU17 PN from 32023VP00-221-G to 320240F00-221-G
P132:Change PU44 PN from 32023VP00-221-G to 320240F00-221-G
P134:Change PU76 PN from 32023VP00-221-G to 320240F00-221-G

20160523 DC

Modify Power sequence as EE request
P141: add PR2197 to pull high to +3P3V

20160523 EE

P079: Add GPI_USB_INT_CABLE1_N
P087: Dummy RO249
P097: Add RU670,RU671,GPI_USB_INT_CABLE1_N;modify INT_USB connector

20160527 EE

P103: Change UO8 PIN19 net name form SER1_RI_N to SER1_RI

20160603 EE

P103,P085: Moved RO344 form page85 to page103 and
change the EC_DEBUG1 design for DELL suggest

20160604 DC

P120: Change PR472 from 0_5% to 150_1%
Change PR473 from 150_1% to 0_5%

BOM Chagne 0_1% (0603) to 0_5% (0603)

P138: Change PR208¡BPR217¡BPR664¡BPR673 from 0_1% to 0_5%
P136: Change PR248¡BPR222 from 0_1% to 0_5%
P140: Change PR297¡BPR2102¡BPR2117 from 0_1% to 0_5%
P137: Change PR688¡BPR1998 from 0_1% to 0_5%
P141: Change PR1283¡BPR1284¡BPR1285¡BPR1286 from 0_1% to 0_5%
P139: Change PR1977 from 0_1% to 0_5%
P142: Change PR2138¡BPR2043¡BPR2152 from 0_1% to 0_5%

20160606 DC

Only support SPI mode
P140: Add PR2324 , for GPPA connect to +3P3VAUX test.

20160606 EE

P090: Swap PCIe TX,RX signal;fix BITS284762
P096: Remove USB3.0 re-driver
P098: Add USB3.0 re-driver
P103: Modify KYBD,MOUSE to G/F material
P104: Modify FRONTPANEL material
P109: Modify RH255,RH262,RH272,RH275,RH276,RH292,RH293,RH234,RH215
to +VCCIO_CPU0

20160608 EE

P075,P102: Modify MINISAS_HD screw material
P094,P095,P099: Modify ECU3~ECU6,ECU13,ECU14 material

20160613 EE

P084: RS154 modify to 1
P108: RF257 modify to PROTO,RF83 modify to NI

20160613 DC

Update main source follow SS requirement
P104: Change POWER2 to HM16100-AEP4-4F
P143: Change PQ32 from AOD518 to AOD558
P144: change PQ55,PQ56,PQ80,PQ81 from IRLML6401TRPBF to DMP2305U-7
change PQ53,PQ54,PQ78,PQ79 from NTJD4001NT1G to DMN65D8LDW-7

20160616 EE

P077: Swap ODD_SATA and LOM2 signal sync for M5 X00
P085: Add thermal sensor
P089: Modify RL205 pull high to +3P3V_DSW;RL2 change to 10K;Add CL190
;Remove RL206;fixed power squence timing BT27 BITS286927

P094,P095,P099: Change UU5,UU7,UU19,UU20,UU71,UU73 material by SS
request;Change ECU3,ECU4,ECU5,ECU6,ECU13,ECU14 material

P109: Change QH9,QH10 material by SS request

20160621 EE

P019: Move RH457 to CPU path
P041: Move RH456 to CPU path
P076: Add RS374 follow PDG P249 design
P089: For BITS286927 intel will update PDG spec.We need to revert back

20160628 EE

P089: Modify QL6 material

20160630 EE

P084: Modify TBT1,INTRUDER material

20160702 EE

P075: Modify MINISAS_HD_2_0~MINISAS_HD_5_1 material
P102: Modify MINISAS_HD_0_0~MINISAS_HD_1_1 material
P107: Modify CF9,CF10 to 0.1uF from 1uF;Nuvoton Adel recommend

20160707 DC

P129: Add PR2326,PQ83.
P135: Add PR2327,PQ84
P139: Add PR2325,PQ82
Change TDA21461 to TDA21471
change TPI-1180-181 to TPI14G-181A
change PC2096 form 22nf to 47nf.
change PR108,PR269 from 100K to 121K.
Change PR110,PR271 from 487K to 576K.
P144: PQ33,PQ25 change from FDN340P to DMP2305U-7

20160708 EE

P111: PCB HH P/N change from 0101DDN01-388-G to 0101DDN02-388-G

20160709 EE

P088: FBO5 HH P/N change from 720101L00-015-H to 720105E00-016-H
P106: Modify FAN_FRONT3~FAN_FRONT4,FAN_REAR1,FAN_REAR2 material to 3406A9P00-600-G
P108: Modify PWR_REMOTE material to 3406A9N00-600-G

20160711 EE

P075: CPU hot plug I2C level shift move from MB to backplane
P079,P082: Add GPI_PCH_HS_DET_N,RO450
P085: Rename EC_UART1_DEBUG_TX
P088: Add CPLD_UART_DEBUG_TX
P103: Modify SER_DEBUG1 side component

20160712 DC

P142:change PC1167 to 470nf(0603),add PD32 (dummy)

20160712 EE

P029,P030,P033~P036,P39,P40,P051,P052,P055~P058,P061,P062: Change DIMM silkscreen
numbering to populate outermost channels first

20160713 DC

Fine turn VCCIO setting and cureent sense setting(follow "Horizon_VR_VCCIO" document)

20160714 DC

For all TDA21471 39pin REFIN add one 0.1uf Cap to GND.
PIN37 ID add one 100k resistor(dummy) to GND

20160714 EE

P079: RS109,RS148 change to 0 ohm
P084: Bettery part reference modify to RTC_BATTERY
P092,P093: Modify RA31~RA33,RA64 from short pad to 0 ohm;RA3 change to 0 ohm;
CA18 change to 33pF;Stuff CA15
P095: Add RU672,RU673

20160715 EE

P094,P095,P099: Change USB3_REAR1,USB3_REAR2,USB3_REAR3 material
P104: Add RP16;FRONTPANEL change to RA

20160718 EE

P066,P067: Modify to High BW mode;add an unused output pin to measure phase noise

20160719 EE

P107: Add PCH_DIS,ROM_EN and peripheral component;need apply SPI_3 to W25Q256FVEIQ

20160720 EE

P003: Modify SMBus Block Diagram
P016: Modify Memory Connection Block Diagram
P096: Modify USB3_FRONT1 material

20160721 EE

P026: Del CH34,CH61
P049: Add CH34 for +VDDQ345_CPU0;add CH61 for +VDDQ012_CPU0
P048: Del CH70,CH89
P049: Add CH70 for +VDDQ345_CPU1;add CH89 for +VDDQ012_CPU1
P107: Update SPI_3 library
P110: Pop RO261,dummy RO266

20160720 DC

1.Add PR2346,PR2347 for +5V and +3P3V to GND.
2#change +3P3V_AUX switch only from +3P3V_DSW for solve drop from S0 to S3
3#dummy M357 PR162, PR1596, PR1039, PR1965, PR1981, PR2177, PR2178
4#Reduce +PVNN_AUX_PCH 1pcs buck cap PCE44,+1P05V_AUX_PCH 1pcs buck cap PCE48
5#Unstuff PR2002¡¢PR715¡¢PR2006¡¢PR2005¡¢PR2027¡¢PR2008¡¢PR730¡¢PR729 for leakage
current
6#VR_HOT_N (PR4¡¢PR456¡¢PR131¡¢PR172¡¢PR587¡¢PR628) needed to pull high to +3P3V
7#unstuff PCE1573¡¢PCE26¡¢PCE32¡¢PCE78¡¢PCE94¡¢PCE97¡¢PCE100¡¢PCE102

20160722 EE

P079: Del GPI_USB_INT_CABLE1_N
P097: Modify INT_USB;Del GPI_USB_INT_CABLE1_N
P110: Modify RO297,RO298 pull high to +3P3V

20160725 EE

P105;P106: Modify Fan part reference
P107: Change UF1 to NPCT650JB2YX

20160725 DC

Change VCCSA solution from powerstage to driver + MOSFET

20160726 EE

P092,P093: Add FP_AUDIO1 and peripheral component for Front Audio issue

20160729 DC

Add 1k reisistor PR2357 for "+1P8V_AUX_PCH" to GND.
dummy PC1234 for "+3P3V_AUX"

20160801DC

change TDA21471 VCC pin input resistor from 0 ohm to 1 ohm for saparation noise
dummy TDA21471 REFIN pin to GND 100nFCAP.
chenge PR714 to 33 ohm from 0 ohm

20160801 EE

P102: Change ODD_SATA material.

20160803 EE

P084: Dummy UPI_SLOW_MODE
P111: Modify MH13~MH17 material;modify PCB size

20160804 EE

P084: Modify RTC_BATTERY_1 material

20160808 EE

P066,P067: Modify FBC2,FBC4 material

20160808 release bom

MATIRA7_EZBOM_X01_0.2_BOM_20160808(compared).xls

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X00 to X01 modify list

20160809 EE

P079: Dummy RS369
P085: Modify UO_EC HH p/n

20160812 EE

P085: Dummy RO364
P097: Modify ECU8_ECU11 HH p/n
P102: Modify ODD_SATA HH p/n

20160820 DC

P123:Dumy PR276
P140:Dumy PR910,PR911,PR2115,PR705,PR703 Stuff PR2324
P142:Change PR743 to 10.7K from 10K ,chang PR746 to 2.32K from 2K
dumy PC1167

20160820 EE

P066,P067: Modify FBC2,FBC4 HH p/n

20160822 EE

P079: Dummy RS371

X01 to X02 modify list

20160901 EE

P078,P079: Move FM_CPU1_SKTOCC_LVT3_N net name to GPP_D11
P079,P087: Add PCH_TCM_DISABLE_N net name,add RS377
P079,P104: Add POWERSHARE_EN_N net name,add RS229
P098: Add RU674
P107: Add China_TPM 2.0
P079,P107: Add PCH_TPM_DET net name
P078: Add RF472,CF107,CK_24M_66M_TCM

20160901 DC

P112: Delete PR34,PR35
P120: Delete PR486,PR487

20160906 DC

P116: Add PR2358,PR2359
P124: Add PR2361,PR2362

20160908 DC

P139: Remove NO_DEEP1 jumper from across PQ41.
Place it between PCH_DEEPSLEEP_N and +3P3V_DSW.
Change PR938 to 20K.
Add PR2360
P143:chang PR805 to 20K.

20160908 EE

P084:Populate RS112,RS110,RS115.Depop RS111,RS113,RS114
P085,P110:Add RST_I2C_PCA9546_N

20160912 EE

P085:Add EC_DEBUG connector

20160913 DC

P142:PR2179 unstuff
add PR2401,PR2402,PR2403,PC2201

P139:Change PR2360 to 100 ohm from 1K ohm
P140:Unstuff +PGPPA_AUX_PCH VR
P141:Add PD34

20160914 EE

P076:Modify RS5 to 1.2k ohm from 0 ohm
P085:Modify fan control signal
P087:Add G6,H1,J3,J4,J5,K2,K6,L10 for fan control
P088:Move net name PWRGD_CPU0_DEF_DRAM_GTL from K12 to G15;
add A3,A4,F15,F16,G11,H12 for fan control

P105,P106:Modify fan control signal

20160920 EE

P069:Modify SLOT2 to black color,dummy SLOT2_LATCH1
P070:Dummy SLOT4_LATCH1
P071:Dummy SLOT6_CPU1_LATCH1
P078:Add RF479,CF108
P088:Add net name PCH_SPKR
P107:Modify TPM co-lay SPI and LPC bus
P108:Modify BUZZER schematic

20160921 EE

P085:Move PCH_SLP_S3_N from EC.F8 to EC.C11;Disconnect PWRBTN
signal from EC.D5.Instead change RO29 to 100K PU to V_3V_VBAT_EC

P092:Del CA105,CPLD_SPEAKER
P106:Reserved resister for fan control signal
P107:LPC_LAD1_ESPI_IO2_TCM rename to LPC_LAD2_ESPI_IO2_TCM.
LPC_LAD1_ESPI_IO3_TCM rename to LPC_LAD3_ESPI_IO3_TCM.

P108:Add PA1

20160922 EE

P098:Remove USB3.0 Re-driver
P111:Modify PCB version

20160923 EE

P107:Add China_TPM_EN connector,RF484;depop SPI_1,SPI_SOCKET_1;
pop SPI_3

20160926 EE

P084:Modify RS111, RS110, RS114, RS79, RS80 to 1K ohm

20160929 EE

P107:Pop SPI_1,SPI_SOCKERT_1,depop SPI_3,due to factory can't burn WSON8

20161005 EE

P085:Modify RO487,RO489,RO491,RO493 from 0 ohm to 4.7K ohm

20161006 EE

P075:Modify FLEX0_0 ~ FLEX3_CPU1_1 total 8 pcs material
P094:Modify UU8,UU55 material
P095:Modify UU56,UU57 material
P097:Modify UU60,UU61 material
P099:Modify UU70,UU72 material
P102:Modify SATA0_0 ~SATA1_1 total 4 pcs material

20161007 EE

P076:Modify RS5 material

20161011 EE

P092:Pop RA29,depop RA30

20161013 DC

P141:Modify PR714 to 10K from 33

20161017 EE

P076~P082:Modify PCH to B1 version
P085:Dummy RO434,RO435,RO436

X02 to X03 modify list

20161005 EE

P084:Del PW_CMOS_SERVICE;add PSWD,CMOS_CLR,SERVICE_MODE

20161012 EE

P079:Add GPP_J2,GPP_J3
P084:Add Air Shroud Dectection Switch

20161013 EE

P096:Modify FP_USB3_1 material
P106:Modify QO20B pin B net name to FAN_PWM_F1_P5

20161014 EE

P025:Dummy CPU0_PC,CPU1_PC
P084:Modify VROC_KEY material

20161018 EE

P107:Depop SPI_1,SPI_SOCKET_1; pop SPI_3

20161026 EE

P075,P102:Modify MiniSAS connector screw
P085:Modify UO_EC to MEC5105K-D2-TN from MEC5105K-D1-TN

20161031 DC

P142:change PR2160 From 7.5K to 5.1K
change PR2161 from 7.5K to 5.1K

20161031 EE

P079,P104:Add HDD_TEMP_DET5#
P111:Modify PCB version

20161104 DC

P111:Change PQ53,PQ54,PQ78,PQ79 from DMN65D8LDW-7 to DMN62D0UDW-7

20161107 EE

P079:Add RS381
P089:Modify QL6 material
P093:Del FP_AUDIO1 and peripheral component
P103:Modify QO1,QO2 material from DMN65D8LDW-7 to DMN62D0UDW-7
P109:Modify QH9,QH10 material from DMN65D8LDW-7 to DMN62D0UDW-7

20161108 DC

P143:Change PQ31 to AON7407 from SISS27DN-T1-GE3

20161109 EE

P107:Stuff SPI_1,SPI_SOCKET_1; depop SPI_3

20161110 DC

P136:DUMY PR237,PR220
P137:DUMY PR657,PR1989

20161110 EE

P094:Modify UU8,UU55 material
P095:Modify UU56,UU57 material
P097:Modify UU60,UU61 material
P099:Modify UU70,UU72 material

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20161115 EE

P076:Modify CS1,CS2 to 15pF;modify CS3,CS4 to 8.2pF
P084:Modify Board Revsion ID from 010 to 011
P085:Modify CO24,Co25 to 22pF
P089:Modify CL7,CL8 to 27pF
P090:Modify XL2 material;CL151 to 12pF

20161117 EE

P105:Add 5 pin CPU fan connector and peripheral component

MATIRA7_EZBOM_X03_0.2_BOM_20161121.xls

20161122 EE

P075:Modify FLEX0 to FLEX0_P0,FLEX1 to FLEX0_P1,
FLEX2 to FLEX1_P0_CPU1,FLEX3 to FLEX1_P1_CPU1

P092:Add RA74;dummy RA27,QA4
P076~P086:Modify US1 to intel EY82C621 QM1Q material

RA30 if need stuff????

20161122 EE

P141:Change PR718 from 86.6K to 169K
change PR713 fome 169K to 243K

20161123 EE

P094,P095,P097,P099:Modify RU454,RU455,RU457,RU470,RU465,RU634,RU652 to +5V_USBKB

20161125 EE

P078:Dummy RS101

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20161129 EE

P075:Dummy UX2,UX3,UX4,UX5 Stuff RX52,RX53,RX54,RX55
P084:Dummy AIR_SHROUD,RS378,RS379,RS380

X03 to X04 modify list

20161201 EE

P075:Dummy RX112,RX113,RX114,RX115;add RX127,RX128
P084:Modify BOARD_REVISION_ID to 0b100 from 0b011
P104:Modify POWER_CTRL_SMBus to I2C_PCIE_MUX from I2C_SM_PCH
P111:Dummy SPI_1,SPI_SOCKET_1;Stuff SPI_3
P111:Modify PCB version to X04

20161202 EE

P075:Dummy QX1,QX2,QX3,QX4,RX85,RX86,RX87,RX88
P085:Modify RO439,RO440 pull high to +3P3V_AUX from +3P3V_AUX_SLOT

20161207 EE

P079:Dummy RS371
P093:Stuff RA13,RA54,RA55,CA85,UA2

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20161212 EE

P093:Modify RA54,RA55 to 0 ohm from 100 ohm

X04 to P01 modify list

20161214 EE

P085:Dummy RH288,RH289,RH290,RH291;modify SPI_2 to SMD
P107:Separate two bom for TPM and China TPM

MATIRA7_EZBOM_P01_0.1_BOM_20161214(compared).xls

20161222 EE

P090:Modify XL2 material
P093:Modify DA8,DA6 from proto to I;Modify DA9,DA11 from proto to NI

P01 to X05/A00 modify list

20170111 EE

P084:Modify SERVICE_MODE from I to PROTO;modify BOARD_REV_ID [2 : 0] from 100 to 101
P084,P105:Modify FAN_CPU0_1,FAN_CPU1_1,TBT material from G/F to Tin
P088:Modify CO85 from PROTO to I
P093:Dummy UA2,RA13,RA54,RA55,CA85
P096:Modify FP_USB3_1 vendor
P097:Modify USB2_FLEX material from G/F to Tin
P103:Modify KYBD,MOUSE material from G/F to Gold 30u.
P106:Modify FAN_SYS2,FAN_REAR1,FAN_SYS2,FAN_SYS0,FAN_REAR0 material from G/F to Tin
P108:Modify PWR_REMOTE material from G/F to Tin;modify RNA1 to 330 ohm
P111:Modify PCB version

20170117 EE

P084:Modify CMOS_CLR to CMOS
P087:Add GPI_INTRUDER_CABLE_DET_N to CPLD_P13, PB25B
P106:Modify UO17,UO18,RO357,CO137,CO141,RO433,RO500 from PROTO to NI
P109:Add RH459,RH460,RH461,RH462

20170118 EE

P079:Modify RS255,RS256 from MP to NI
P088:Modify DO3,RO195,RO201,RO205,RO203,CO84 from PROTO to I

20170123 EE

P087:Add CO150,CO151

20170124 EE

P087:Modify CO150,CO151 from 0.1uF to 0.01uF

20170206 DC

P114:Modify VR_HEATSINK_CPU0 from I to NI

20170216 EE

P085:Change SPI_2 from SMD Type to DIP Type
P111:Change PCB P/N from 0101DDN06-388-G to 0101DDN07-388-G
P111:Change PCB Description

20170301 EE

P108:modify LBL1 reference to BIOS_LABEL and add footprint:LABEL_10X10
P085:modify Q027,Q028,QO30,QO31 footprint follow factory sugguestion

20170301 DC

P139:PR2360 change from 100 ohm to 1K

20170302 EE

P094:Modify RU34,RU35 schematic and value
P095:Modify RU69,RU71,RU676,RU677 schematic and value
P097:Modify RU666,RU678,RU694,RU679 schematic and value,modify USBPWR_7_F net to USB2_INT_PWR
P099:Modify RU633,RU647 schematic and value
P111:Change PCB P/N from 0101DDN07-388-G to 0101DDN06-388-G

20170310 EE

P075:Modify FLEX0_P0 --> PCIE0,FLEX0_P1 --> PCIE1,FLEX1_P0_CPU1 --> PCIE0_CPU1,
FLEX1_P1_CPU1 --> PCIE1_CPU1

P107:SPI_3 modify to NI;SPI_1 modify to W25Q256JVFIQ;SPI_SOCKET_1 change to PROTO

20170315 EE

P097:Modify USB2_FLEX to Gold Flash
P108:Modify BIOS_LABEL footprint

20170316 EE

P078:Add RF485,RF486,RF487
P079:Add RS384,RS385;modify RS290,RS291 to 402 ohm from 10k ohm
P080:Add RS382,RS383,QS8,QS9
P088:Add net PCH_SUSWARN_N,PCH_SUSACK_N,RO536,RO537
P076~P082:Modify US1 PCH to QM1X from QM1Q

20170323 EE

P078:Modify RS27 to NI from I
P111:Modify MH13~MH17 package type to SMD from DIP

20170324 EE

P078:Depop RF485,RF486,RF487
P079:Depop RS384,RS385;modify RS290,RS291 to 10k ohm from 402 ohm
P080:Depop RS382,RS383,QS8,QS9

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P01 to X05/A00 modify list

20170327 EE

P085:Pop RO124;SPI_2 change to SMD
P107:SPI_1 change to SMD
P108:Remove BIOS LABEL
P111:Modify PCB Version

20170405 EE

P093:Modify SPKR_INT to tin from Gold Flash
P103:Modify KYBD,MOUSE to Gold Flash from Gold 30u

P111:Modify PCB vendor P/N

20170405 DC

P136:Change PU23,PU24 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z
P137:Change PU56,PU81 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z
P139:Change PU25 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z
P140:Change PU26 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z
Change PU49,PU50 from MPQ8623GD-Z to MPQ8623GD-C783-Z

P142:Change PU54,PU70 from MPQ8623GD-Z to MPQ8623GD-C783-Z
Change PU52 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z

20170407 DC

P140:Change PU49,PU50 footprint to QFN_14_20_79X118
P142:Change PU54,PU70 footprint to QFN_14_20_79X118

20170411 EE

P096:Modify FP_USB3_1 to Gold Flash from Gold 15u

20170510 EE

P025:Modify CPU0_BSDC,CPU1_BSDC foxconn P/N
P076~P082:Modify US1 foxconn P/N

20170516 EE

P111:Modify PCB vendor p/n from 08EA25C48K to 08EA25C48L

20170607 EE

P079:Depop RS365

20170629 EE

P085:Add @SPI_2 for EC FW
P087:Add @UO1 for CPLD FW
P090:Add @UL3 for LAN2 FW
P107:Add @SPI_1 for BIOS FW

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